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Test & Measurement World

THE MAGAZINE FOR QUALITY IN ELECTRONICS

Scott Wood, test-engineering manager at Polycom.

BOUNDARY SCAN STARS IN HD CONFERENCING

Engineers at Polycom chose IEEE 1149.1 JTAG technology to ensure the testability of their company's new high-definition videoconferencing system.

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COVER BY: DAN BRYANT

Test & Measurement World

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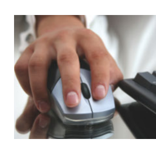

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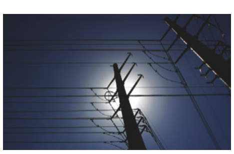

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Guest commentary

PCI Express, multicore processors, and FPGAs drive Instrumentation 2.0

Test instrumentation is undergoing a fundamental change—from fixed-functionality stand-alone instruments to flexible software-based devices that users can redefine. Eric Starkloff, director of product marketing at National Instruments, comments on how the change parallels the emergence of user-empowering Web 2.0 technology.

www.tmworld.com/guests

Spectrum analyzers: product comparison

As a companion to "Spectrum analyzers respond to digital modulation," which appears on p. 45 of this issue, we have compiled a Web-exclusive chart that compares the features of currently available 2.5-GHz and up spectrum/signal analyzers.

www.tmworld.com/product_chart_sa

Blog commentaries and links

Rowe's and Columns

Martin Rowe, Senior Technical Editor

- Review: Agilent U1604A oscilloscope
- Review: Protek 860F oscilloscope
- Review: Fluke 199C ScopeMeter
- Review: AEMC OX 7104-C oscilloscope

Taking the Measure

Rick Nelson, Chief Editor

- Offshoring's temporary setbacks
- Marketers give engineering its due
- Electron pushers face offshoring

Education and Careers

Amy Laskowski, Contributing Editor

- Everyone can be a computer programmer!
- Educational cycling

www.tmworld.com/blogs

Take a T&M Challenge

Respondents who answer one of our T&M Challenge questions correctly are entered into a drawing for a prize, courtesy of the contest sponsor. Current prizes are an Apple iPod and Bose Noise-Cancelling headphones. New challenge questions every month!

www.tmworld.com/challenge

Offshoring's inevitability

Will offshoring inevitably lead to a catastrophe for workers in developed companies? Columnist Robert J. Samuelson writing in the *Washington Post* (May 16, p. A15) says no—fears that white-collar work would be zapped around the world are overblown. In fact, he writes, only 4% to 5% of mass layoffs in the US and Europe have been due to offshoring, because offshoring is not easy to do: Problems include culture and language differences, lack of skilled workers, and customer complaints.

But also writing in the *Post* (May 6, p. B04), Princeton economics professor Alan S. Blinder is less sanguine.

RICK NELSON, CHIEF EDITOR

"I'm a free trader down to my toes," he writes, but nevertheless cautions that "the offshoring of service jobs from rich countries…to poor countries…may pose major problems for tens of millions of American workers over the coming decades." He cites research showing that 30 million to 40 million US jobs are potentially offshorable. And Samuelson concurs that "As communications technology improves…offshoring may increase."

There have been notable offshoring failures. They are difficult to track down, because companies are reluctant to report their mistakes. The technology consultancy ebs (www.ebstrategy.com), however, has cataloged some of them, including Dell's abrupt turnabout on outsourcing corporate technical-support call-center work because of customer complaints.

> **Engineering may be easier to offshore than call-center work.**

But I think such turnabouts will increasingly become the exception. The rule will be represented by the success Polycom's Austin-based engineers have had—as I recount in this issue's cover story—in delegating test-engineering responsibilities to Thai engineers who work for Polycom's Asian contract manufacturer. Those Thai engineers, by the way, were educated at UT Austin.

In fact, engineering, with its relatively rigid degree requirements, may be easier to offshore than call-center work. Call centers are unlikely to invest much more in worker training than ensuring minimal language skills. It may be cheaper (if you are serving an English-speaking clientele) to hire native English speakers who can appease disgruntled customers whose problems defy a scripted solution. An engineer's skills, however, do not depend on his or her native language.

Blinder offers no suggestions for minimizing offshoring's potentially nasty effects, but says he is speaking out because, "If we economists stubbornly insist on chanting 'Free trade is good for you' to people who know that it is not, we will quickly become irrelevant to the public debate."

We developed-world workers will all have to engage in that debate as we strive to innovate to maintain our relevance in the face of ever-increasing offshore competition. T&MW

Post your comments at www.tmworld.com/blog.

BRAD THOMPSON
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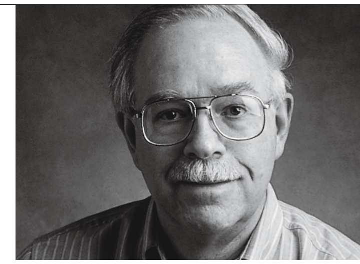
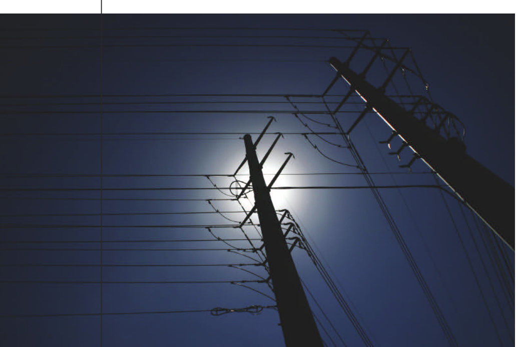


Night thoughts

At 3:22 a.m. the lights went out, triggering the alarms on our household PCs' UPSs and startling our cat, who launched himself from the bed and awakened me. After silencing the alarms and soothing the cat's jangled nerves, I lay awake thinking night thoughts and listening to the storm's winds howling through the pines and the sleet ticking on the windows.

Were we ready for a prolonged power outage? I hadn't tested our standby generator in months, and the transfer switch I bought a few years ago languishes in its carton awaiting installation. And were we ready for a larger emergency that would force us to relocate our household for a few days?



Hearing tree branches snapping in the wind, I wondered whether the telephone and coaxial-cable lines would escape damage. As a society, we've grown dangerously dependent on instant communications via cell phones, which in turn rely on AC power sources to recharge their batteries and operate the cell sites. While wired-phone service offers greater resilience, mechanical damage can disrupt its lines. An amateur-radio "go package" comprising a low-power multiband transceiver, a high-capacity gel-cell battery, and basic antennas could provide emergency message-relay service, but as of yet, I haven't assembled one.

I arose, disturbing the cat again as I stumbled into the bathroom for aspirin and a glass of water. If the semiconductor industry ran on pharmaceutical models, we'd still be using 7400-series TTL as "glue" logic for the latest systems-on-a-chip. We'd test semiconductors by building products, device data sheets would appear in two-point typefaces, and no design engineer would ever pay for lunch again.

The aspirin helped me drift off to sleep, only to awaken too soon at the usual time thanks to a battery-powered clock radio. A propane camp stove provided hot water for coffee, and our wood stove provided a modicum of warmth. Later, I would spend several hours patch-wiring the generator into the house power panel (after locking out the service-entrance circuit breaker) and using the car to jump-start the generator. AC power would return several hours later, and data service a few hours after that.

We were lucky. The storm inflicted only minor inconveniences on our household, while other parts of New Hampshire experienced 100-year flooding for the second year in a row. I gave my personal disaster-response readiness a grade of C-minus. What's yours? What's your company's? T&MW

INSTRUMENTS OF DISASTER, REVISITED

For *Test & Measurement World*'s December 1993 issue, I wrote an article entitled, "What to Do When Disaster Strikes." After reviewing its contents, I wouldn't change its basic premise and conclusions, except to note that given the PC's ever-increasing penetration of the test lab, program and data backup and offsite storage have become even more important than they were over a decade ago.

You can read a PDF of my 1993 article in the online version of this article: www.tmworld.com/2007_06.

While cell phones can serve as indispensable emergency personal-communications devices, they're also a slow-moving disaster in their own right. According to Giles Slade, author of "*Made to Break: Technology and Obsolescence in America*," in 2005, Americans retired approximately 50,000 tons of cell phones, most of which went into landfills and incinerators.

If the prospect of nickel-cadmium battery waste released into ground water or the air you breathe doesn't make you nervous, it should. You can learn more about the book here: www.hup.harvard.edu/catalog/SLAMAD.html.

For a look at a fascinating aspect of obsolescence that's not familiar to most engineers, visit "A Secret Landscape: America's Cold War Infrastructure," a Web site that describes facilities and structures that played a role in preventing the ultimate disaster—a nuclear war between the US and the USSR. Here, you can visit Wullenweber and "elephant cage" antenna sites and abandoned facilities and learn about AUTOVON and AUTODIN.

While you read, remember that every antenna and piece of equipment underwent extensive electronic tests: coldwar-c4i.net/index.html.

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The N6705A integrates the capabilities of up to four power supplies, a DMM, an arbitrary waveform generator, a scope, and a data-logger into a single instrument.

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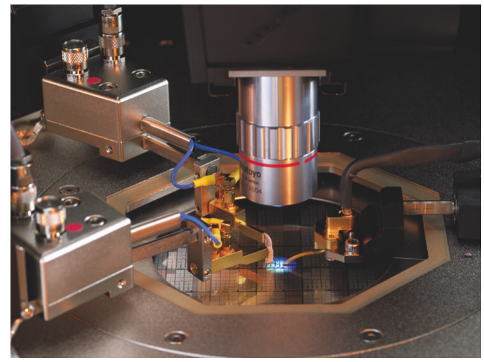
Tesla power-semiconductor characterization system debuts



Cascade Microtech has announced its new Tesla characterization system, which performs on-wafer probing of power semiconductors at levels to 60 A or 3000 V. Cali Sartor, senior product manager at Cascade, said the new system takes aim at a worldwide power semiconductor market that's projected to grow from $25.8 billion in 2007 to $34.2 billion in 2009, according to Yole Développement (www.yole.fr). Burgeoning demand for power devices, Sartor said, puts time pressure on power-semiconductor engineers and test technicians who can no longer afford the time and expense of packaging their devices to perform characterization and model extraction.

Tesla features two new wafer probes, including a high-current probe that can support 10 A in continuous mode and up to 60 A in pulsed mode. To reduce device heating, the probe tip minimizes contact resistance at the wafer-to-probe interface. The Tesla system also features a high-voltage probe that can make coaxial measurements up to 3000 V and triaxial measurements up to 1100 V. Both the high-current and the high-voltage probes feature a replaceable tip. The Tesla system's wafer chuck employs a chuck-top technology that optimizes vacuum levels to protect against wafer breakage and probe damage while ensuring minimal contact resistance. Base price: $200,000. www.cascademicrotech.com.

Test summit scheduled for Semicon West

At the SEMI Test Summit & Reception at Semicon West in San Francisco, executives from five semiconductor ATE companies will join moderator Rick Nelson, chief editor of *Test and Measurement World*, and host Ashoke Seth, test operations director at Intel, in a discussion focused on meeting the design, test, and yield requirements for advanced semiconductor manufacturing. Panelists will include R. Keith Lee, president and CEO, Advantest America; Lavi Lev, CEO and president, Credence Systems; Tim Moriarty, president, Nextest Systems; Mark Jagiela, president, Teradyne Semiconductor Test Division; and Keith L. Barnes, president and CEO, Verigy.

The summit will take place Wednesday, July 18, from 5:30 p.m. to 7:00 p.m. at the Moscone Center, West Hall, Level 2. A reception will follow the panel discussion. semiconwest.semi.org.

Open-Silicon adopts Synopsys DFT MAX

Synopsys has announced that Open-Silicon has adopted Synopsys' DFT MAX scan-compression technology to reduce the cost of testing its 130-, 90- and 65-nm ASIC designs while having minimal impact on Open-Silicon's established design flows. Using DFT MAX within its existing Synopsys Galaxy Design Platform flows, Open-Silicon's design team achieved a 90% test-application-time reduction for scan testing.

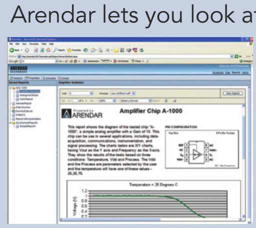
Working within the Galaxy platform, DFT MAX avoids the need for fragmented, bolt-on flows requiring separate design-synthesis and test-

Editors' CHOICE

Investigate and report test data

Arendar 2007 from VI Technology pulls together test data from automated test systems across a network. Arendar is enterprise software that helps users "investigate" data through math operations and then format the data into publishable reports.

Arendar works through a Web browser. As an investigative tool, Arendar lets you look at data across multiple parts and across multiple test conditions. You can use "and" and "or" operations to uncover trends or anomalies in test data, then use charts such as histograms and Pareto charts to plot results.



As a reporting tool, Arendar 2007 pulls data from a database using report templates that include text, data, and graphics. Templates let you develop custom reports for individual devices or generate reports for a set of devices. An export function lets you publish reports in HTML or PDF formats. You can schedule reports through a scheduling wizard and receive reports at specified time intervals. You can also create your own applications, because Arendar's programming interface is accessible from any .NET language.

Prices: processor-model—$38,995 per processor with no user licenses needed; client-server—$15,000 per server and $1000 per client. *VI Technology, www.vi-tech.com.*

compression insertion steps that can break critical timing, add routing congestion, and necessitate subsequent re-optimization.

"Optimizing costs is a key element to the success of our OpenMODEL services," said Dr. Satya Gupta, VP of engineering at Open-Silicon. "We carefully evaluated many different aspects of the Synopsys DFT MAX scan compression solution, from the way it performed with different compression parameters to its effect on downstream flows and fault coverage. In all aspects, DFT MAX produced results to our satisfaction: the tool substantially reduced test time and test data volume with very low gate/routing area and timing impact." www.open-silicon.com; www.synopsys.com.

Suss MicroTec opens Singapore applications center

Suss MicroTec has opened a facility in Singapore that will provide application support for customers in the Asia-Pacific region. The facility combines the various technologies needed for the accurate characterization and modeling of MOSFET, CMOS, RFIC, MEMS, and optosemiconductor devices, including high-brightness LEDs and imaging sensors. The facility can perform I-V, C-V, noise, S-parameter, and other semiconductor parametric measurements. www.suss.com.

CALENDAR

EMC Symposium, July 8–13, Honolulu, HI. Sponsored by IEEE, EMC Society. *www.emc2007.org.*

Semicon West, July 16–20, San Francisco, CA. Sponsored by SEMI. *www.semi.org.*

NCSL International Workshop & Symposium, July 29–August 2, St. Paul, MN. Sponsored by NCSL International. *www.ncsli.org.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Editors' CHOICE

Sony debuts 5-Mpixel camera

Sony Electronics has unveiled its first 5-Mpixel digital machine-vision camera—the XCL-5000 addition to Sony's Camera Link series. The company reports that the camera can help manufacturers and integrators improve their system design capabilities by using one higher-resolution camera instead of multiple lower-resolution cameras for large part inspection applications, including printed-circuit-board and display inspection. Reducing the number of cameras simplifies designs and lowers costs, while providing streamlined image processing and higher throughput.

The black-and-white XCL-5000 incorporates a new ⅔-in. progressive-scan CCD sensor with square pixels. It can capture high-resolution video at 15 fps, and it supports up to 12-bit processing with a C-mount lens. Connectivity takes place through a standard Camera Link MDR 26-pin connector. Integrated digital-signal-processing capabilities give users options for tailoring systems for optimized performance in customized applications.

Integrated DSP capabilities address gamma correction and support lookup tables. The unit measures 44x44x57.5 mm.

Base price: $4377. *Sony, www.sony.com/videocameras.*

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Year of the mixed signal

2007 isn't half over, but I'm already declaring it "The year of the mixed signal." Yokogawa, Tektronix, LeCroy, and Rigol introduced mixed-signal oscilloscopes (MSOs) or mixed-signal options for existing oscilloscopes this year. The four join Agilent Technologies in the MSO market.

Yokogawa was first with the DL9710L. Released in February, this instrument has four analog channels and 32 logic channels. In March, LeCroy countered with 18- or 36-channel logic options for its WaveRunner Xi and WaveSurfer Xs two- and four-channel oscilloscopes. (The company had previously offered a USB-based logic-analyzer accessory.)

In April, Tektronix reentered the MSO market when it introduced the MSO4000, which has two or four analog channels and 16 logic channels. Rigol's four models in the DS1000CD series have two analog and 16 digital channels.

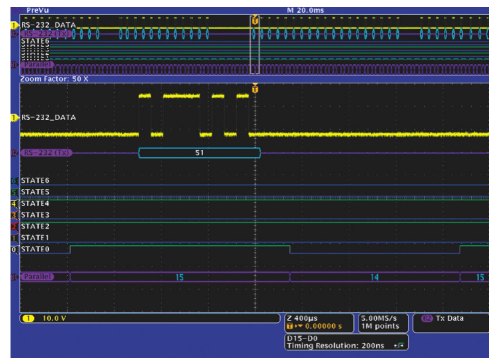
So many MSOs recently appeared because just about everything has an embedded processor, a field-programmable gate array (FPGA), an analog-to-digital converter (ADC), or a digital-to-analog converter (DAC). Devices that had previously relied on mechanical or analog control now use digital logic.

Applications for digital devices vary widely, from refrigerators to levelers that use lasers to align wall pictures. Popular applications include consumer products such as MP3 players and automotive engine controllers. Even power supplies include digital controls.

In many engineering labs, mixed-signal oscilloscopes eliminate the need for dedicated logic analyzers. "Engineers may have a logic analyzer on a cart and use it once in a while," said Chris Lohberg, product manager at Tektronix, "but the oscilloscope is always on."

Agilent has offered MSOs with 16 digital channels for several years. Yokogawa chose to double that number because, according to product manager Joseph Ting, many engineers are developing embedded systems with 32-bit processors.

LeCroy chose to offer 18 and 36 logic channels because "engineers working on 16-bit and 32-bit processors need the extra channels for clock and control signals," said product manager Dan Monopoli.



Mixed-signal oscilloscopes can decode serial data streams such as RS-232. Courtesy of Tektronix.

Engineers who develop systems with parallel buses often use the "bundling" feature to simplify displays. With bundling, you can group signals into one "bus" and display the value in numerical format (usually hexadecimal). If you see an incorrect value, you can expand the bundled signal into its components and troubleshoot individual signals.

MSOs now include the ability to decode serial buses in addition to parallel buses. "MSOs combine an oscilloscope with a logic analyzer and a protocol analyzer," said Ting. The ability to decode serial buses such as Inter-IC (I2C), RS-232, local interconnect network (LIN), and controller area network (CAN) is included in the latest mixed-signal oscilloscopes.

The **figure** shows an MSO decoding an RS-232 signal into its digital value. With their decoding capability, MSOs can now trigger an acquisition based on a serial-bus value. They've always been able to trigger on a parallel-bus value. T&MW

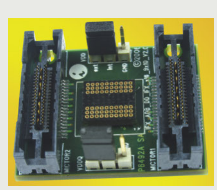
App note describes data streaming

Strategic Test has released an application note that describes how to stream data to or from a hard drive and its PCI digitizer or arbitrary waveform generator cards. "Optimising the transfer rates for UF2 cards" explains how to set up a host computer to achieve data rates of over 200 Mbytes/s. www.strategic-test.com/library.

Case studies show uses of data-acquisition cards

Microstar Labs has published several case studies that show how engineers use its data-acquisition cards. Applications include aircraft materials measurements, vibration analysis, and sound-quality measurements. www.mstarlabs.com/apeng/casestudies.html.

Adapter probes digital circuits



The PB-BGA60C-DDRRAM-RIGID-01 logic analyzer adapter lets you use Agilent Technologies' 16XXX logic analyzers to perform memory-device analysis on devices used in PDAs, cell phones, digital cameras, and MP3 players. The connector consists of a base that you solder to a printed-circuit board (PCB) and a probe board that you connect to your logic analyzer. Price: $1050. www.ironwoodelectronics.com.

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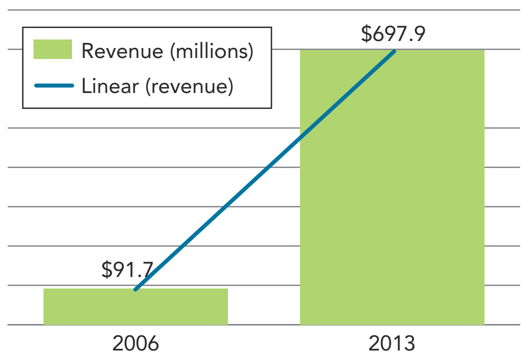
Quality of Experience and triple-play test equipment

"TRIPLE PLAY" HAS BEEN a buzzword in the telecommunications industry since 2005. With fixed-mobile convergence as the major technological trend in the industry, the main focus is to develop next-generation networks that combine data, voice, and video applications over a single platform. If a test-equipment vendor currently provides an IPTV test system, it is a given that the vendor will eventually have to offer a solution that tests voice and possibly data traffic as well.

VoIP and IP video test-equipment vendors have started to offer triple-play test and monitoring solutions. While a large number of test-equipment vendors offer some degree of integration, only a limited number of companies, including Ixia, Spirent Communications, and Shenick Network Systems, currently provide an integrated triple-play test solution that tests voice, video, and data services on a single converged platform.

According to research we have performed at Frost & Sullivan, the integrated triple-play test-equipment market registered revenues of $91.7 million in 2006. This market is expected to reach $697.9 million in 2013 with a compound annual growth rate of 33.6% from 2006 to 2013.

The growth of the triple-play market is mainly attributed to the growth of IP video deployments. IP video gained significant acceptance in the telecom market in 2004 and has been one of the driving forces in the triple-play market ever since. The benefits IPTV offers are significant, including the capability to deliver more channels, faster shifting between channels, picture-in-picture display for programming guide, the time shifting of programs, and integrated services such as onscreen caller display if a customer has subscribed to both phone and TV services.



The triple-play test-equipment market will grow from $91.7 million in 2006 at a compound annual growth rate of 33.6% through 2013. Source: Frost & Sullivan.

Apparently, customers are more tolerant of poor voice and data quality than they are of a disruption in video services—if an issue with video quality occurs while customers are watching TV, the end-user experience is greatly affected. As a result, the deployment of IP video technology led telecom providers to begin measuring end-user Quality of Experience (QoE) to ensure they were meeting customer expectations. In turn, the need to measure QoE has also driven growth in the integrated triple-play test-equipment market.

Similar to subscribers' preference for the convenience of one bill for all of their communication and entertainment services, service providers prefer to deal with one test-equipment vendor that can offer an integrated solution that tests and monitors voice, video, and data in one box. This saves them time, money, and space. T&MW

PCB book to bill

The North American rigid PCB industry book-to-bill ratio for March 2007 inched up to 0.99 from 0.96 in February and 0.91 in January, according to IPC. The North American flexible circuit book-to-bill ratio jumped up to 1.18 from 0.97 in February and 0.93 in January. The combined (rigid and flex) industry book-to-bill ratio in March 2007 reflected these gains, increasing to 1.00, up from 0.96 in February. www.ipc.org.

Wireless USB to soar in 2007

The Universal Serial Bus (USB) saw continued success in 2006, but 2007 is going to be a milestone as wireless USB (WUSB) products are expected to hit the market around midyear, reports In-Stat. The initial WUSB products will be dongle and hub solutions that will allow PCs to wirelessly connect to PC peripherals and consumer electronics devices, the market-research firm says. www.in-stat.com.

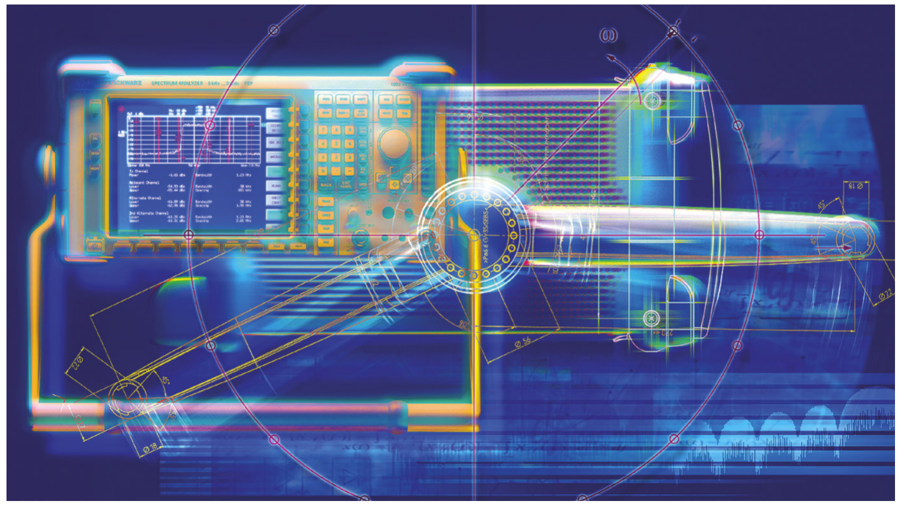
Semiconductor equipment book to bill

North American-based manufacturers of semiconductor equipment posted $1.42 billion in orders in March 2007 (three-month average basis) and a book-to-bill ratio of 1.00, according to SEMI. The three-month average of worldwide bookings in March 2007 was $1.42 billion. The bookings figure is over 1% higher than the final February 2007 level of $1.40 billion and over 2% above the $1.39 billion in orders posted in March 2006. www.semi.org.

Pulsed Signals

The Ultimate Tool for Pulsed Signals

Spectrum analyzers offer engineers the best solution for measuring pulse width, peak power, phase noise and other key parameters

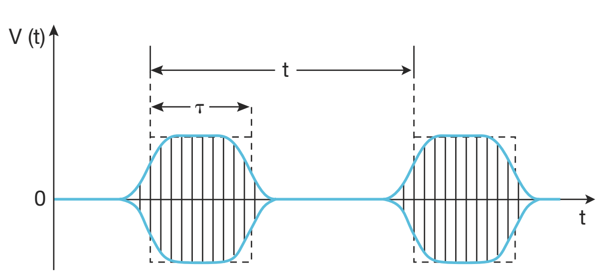


Spectrum analyzers have become essential to engineers who need to take the diverse measurements associated with pulsed signals.

A very large portion of microwave signals involve pulsed modulations. Yet because of the nature and duration of these signals, engineers can face some tough challenges taking essential power measurements.

Successful measurement of RF power flow requires the analysis of many different parameters. Modern radar applications, for example, involve continuously changing pulse parameters. As a result, you can't use a power meter to calculate peak power from mean power. Yet peak power is vital for many reasons, including preventing injuries to personnel from high-power transmission, particularly while a radar antenna is rotating.

At bare minimum, power measurement demands that engineers take into account both the frequency and time domain. Typical measurements on a pulse include: pulse power (peak or average) and pulse shape, usually assessed with an oscilloscope at "video out." You also need a time domain measurement to capture the pulse profile, peak power, average power and a pulse profile – including rise time, fall time, pulse width and pulse period. Still other important pulsed signal characteristics include: carrier frequency, occupied spectrum, carrier on/off ratio, pulse repetition frequency, rise-/fall-time, phase noise and peak power.



A pulsed signal is an RF signal that is switched on and off periodically. Within the RF pulse, the carrier frequency might have additional amplitude/frequency or phase modulation. Important parameters are the pulse width (t) and the pulse repetition interval time (T).

Reach for a Spectrum Analyzer

Fortunately, you can tackle all of these measurements with state-of-the-art spectrum analyzers. These devices display the frequency spectrum or the waveform of a signal in the time domain using a raster scan cathode ray tube (CRT) or a liquid crystal display (LCD). The measurement challenges that you can address include frequency domain, time domain and modulation domain.

In the frequency domain, the typical pulse spectrum is a sin x / x function. The most important parameters to capture are the pulse width (t) and the pulse repetition interval time (T).

The pulsed signal consists of many spectral lines across a wide frequency range. Depending on the pulse parameters and the resolution bandwidth (RBW), you can find three different cases of the spectral result display. If the RBW is smaller than the spacing of the spectral lines, changing the RBW does not change the measured level of the spectral lines. With a bandwidth smaller than the spacing of the first null in the envelope (1 / pulse width), you get an envelope spectrum. Finally, if the bandwidth is wider than the null spacings, the whole spectrum falls within the bandwidth. Result: you can't measure the spectrum of the signal. With a further increase of the bandwidth, the response approaches the time domain function of the pulse.

Depending on the pulse parameters, you can also calculate the pulse desensitation factor, which is the reduction of the level measured within the pulse bandwidth of the spectrum analyzer. In this case, the marker reading plus the desensitation factor would equal the peak power.

For pulsed measurements, the RBW setting is very important. Changing the RBW will lead to changes in the measured level. The pulse desensitation factor now depends on the pulse parameters and the RBW. This is because the bandwidth is greater than the spacing of the spectral lines, and the measured amplitude depends on the number of lines within the bandwidth and the total signal bandwidth.

Furthermore, the pulse desensitation factor depends on the pulse parameters and the RBW. The resolution bandwidth correction factor is driven by the shape of the filter since the bandwidth's shape reflects the power within the filter bandwidth. If the RBW is too wide, the line or envelope spectrum changes to a time domain spectrum, and you can begin to see the impulse response of the RBW filter.

Time and Modulation Domains

With the spectrum analyzer in time domain, you should be able to get a direct measurement for pulse width. The peak marker then allows measurement of peak power, while the delta markers allow measurement of parameters such as rise time, fall time pulse repetition interval and overshoot.

With a wide RBW and video bandwidth (VBW), the spectrum analyzer can track the envelope of the RF pulse so you can see the impulse response of the pulse. The maximum RBW/VBW limits the spectrum analyzer's capability to measure narrow pulses. The general rule of thumb is that for the shortest pulse you can measure, the pulse width is greater than or equal to 2/RBW. But modern spectrum analyzers can exceed these results.

As for other important measurements, radar systems generally use modulation within the RF pulse. Understanding the power characteristics related to this modulation is important since radar range is limited by the available power within the pulse. Conversely, a longer pulse length will lead to limited resolution. Modulation formats can range from simple FM (chirp) to complex digital modulation formats, which modern spectrum analyzers can describe.

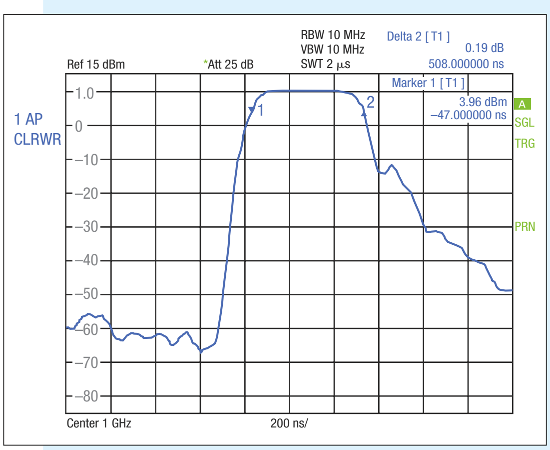
Spectrum analyzers can measure traditional analog modulation in pulse (AM, FM, φM), as well as perform additional analysis functions involving demodulation of all kinds of digital modulation formats, Barker code BPSK modulation within the RF pulse, and pulse-to-pulse phase measurement.

R&S FSU spectrum analyzers are performance leaders in dynamic range, phase noise, level accuracy and resolution bandwidth. Offering a resolution bandwidth from 1 Hz to 50 MHz, the devices can take up to 70 measurements per second (including trace transfer via GPIB).

Power Measurement on Pulsed Signals

The pulse width is the point where the signal level is at 50% of its average voltage across the pulse length. This point is at 6 dB below the peak level in a logarithmic level grid typically used on a spectrum analyzer.

To measure pulse width, set a marker at 6 dB below the average pulse power on the rising edge, and set a delta marker on the point 6 dB below the average power on the falling edge of the pulse. The level reading of the delta marker in this case should be 0 dB. Due to the limited resolution of the measured points, a small level difference has to be accepted. The reading of the delta marker "Delta 2 [T1]" in this measurement shows the pulse width of 508 ns.



The accuracy of this measurement is influenced by the A/D converter sampling rate, which defines the positions within the trace where real measurement values are available. Between these points, the trace data is interpolated to generate the displayed points of the trace.

Analyze with This!

For all these vital measurements of pulsed signals, there is no substitute for a leading-edge spectrum analyzer. Since 1986, Rohde & Schwarz has offered the most innovative spectrum analyzers on the market. Customers from all over the world rely on the accuracy of Rohde & Schwarz spectrum analyzers, for instance the R&S FSU family. These instruments are performance leaders in dynamic range, phase noise, level accuracy, and resolution bandwidth – all essential factors in the design, test and manufacture of next-generation wireless elements.

Rohde & Schwarz is one of the world's leading suppliers of solutions in test and measurement, broadcasting, radio monitoring and radiolocation, as well as mission-critical radio communications. Established more than 70 years ago, the company has a global presence and a dedicated service network in over 70 countries. ●

For More Information

Engineers can learn more about pulsed signal measurement in the R&S Application Note, "Power Measurement on Pulsed Signals with Spectrum Analyzers" at: http://www.rohde-schwarz.com/appnote/1EF48.html

View product specs on Rohde & Schwarz spectrum analyzers at: http://www.rohde-schwarz.com/product/FSU.html

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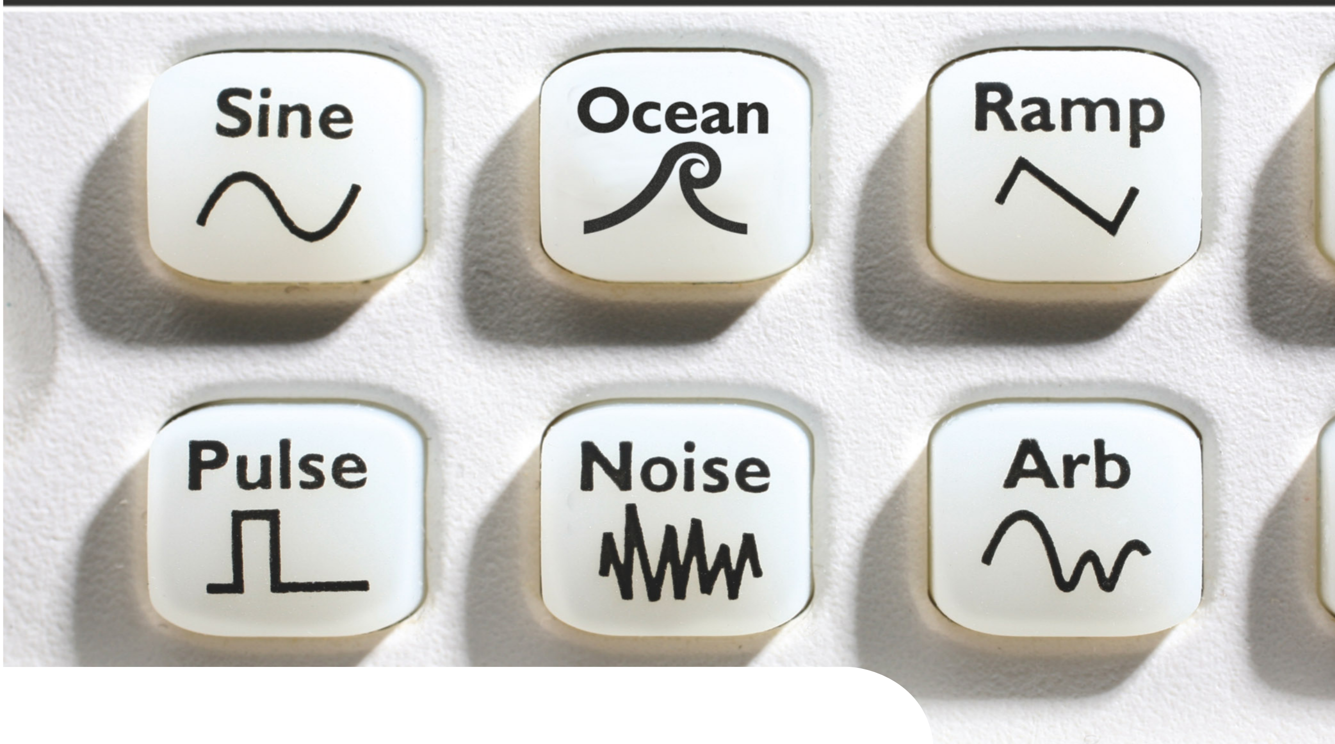

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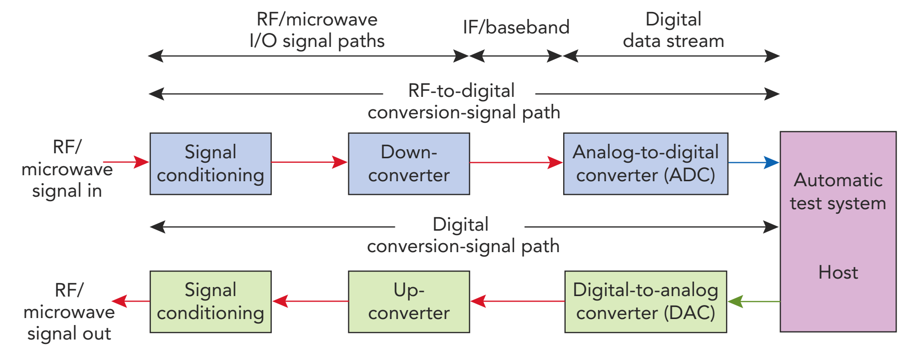
INSTRUMENTS

Understanding synthetic instruments

Synthetic instrumentation (the concept of using a common set of hardware for many test applications) is starting to see implementation in military test applications. The potential gain comes from reducing the risk of test-equipment obsolescence by implementing test functions in software rather than in measurement-specific instruments.



Synthetic instruments use signal conditioners, up/downconverters, and ADCs to convert incoming signals to digital for processing, while DACs convert processed digital signals back to analog.

Mike Granieri of Phase Matrix and Wade Lowdermilk of BAE Systems have written a paper called "The Case for Synthetic Instruments" in which they explain three basic implementations of synthetic instruments:

- *Class A: Modular/loosely coupled open architecture*. A "spin your own" architecture based on modular instruments (ADCs, DACs, and up/downconverters) where test engineers develop their own measurement functions such as rise time, fall time, and frequency entirely in software. This implementation is the most flexible but requires the most effort.
- *Class B: Integrated synthetic instruments*. Here, a manufacturer purchases a test system's hardware and the software that implements measurement functions. A test engineer then develops tests by stringing together measurements. Class B requires less investment in software development than the modular approach, with some limitations.
- *Class C: Application-specific synthetic instruments*. This implementation results in measurements specifically tailored for a specific device under test, but it limits flexibility should a new device require testing.

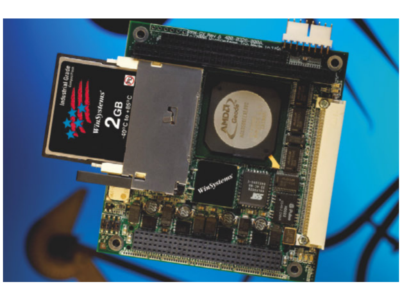
Granieri and Lowdermilk claim that using synthetic instruments "increases measurement speed and testing efficiency" because synthetic instrumentation "is primarily a signal based stimulus & measurement paradigm." They go on to argue that a signal-based method can process a data set faster than a traditional instrumentation setup can and that use of synthetic instrumentation fosters test and measurement interoperability and can reduce training costs. You can download a copy of their paper from the online version of this article (www.tmworld.com/2007_06).

Martin Rowe, Senior Technical Editor

DATA ACQUISITION

M2M gets ready for a trillion sensors

The Internet has revolutionized personal and business communications, and TCP/IP and other communications protocols stand ready to do the same for embedded computers, which increasingly are communicating with other computers and myriad sensors over machine-to-machine (M2M) links.



The PPM-GX, a PC/104-Plus compatible single-board computer, sports an Ethernet controller, four UARTs, and two USB ports. Courtesy of WinSystems.

That's the contention of Bob Burckle, VP of WinSystems, who at the April Embedded Systems Conference (ESC) in San Jose, CA, detailed his firm's plans to take advantage of the market potential of M2M. A key driver, he said, is the proliferation of sensors, which, according to research from the Focal Point Group, could number 1 trillion by 2010, when they will complement 500 billion microprocessors, 2 billion smart devices (including appliances, machines, vehicles, and building equipment), 1 billion handheld smart devices (including mobile phones and PDAs), and 300 million personal computers.

Burckle said WinSystems aims to address this market with single-board computers that can process sensor data and communicate it over a variety of communications links, including Bluetooth and Ethernet as well as CDMA and GSM cellular links. The company's latest offering, introduced at the ESC, is its PPM-GX, a PC/104-Plus com-

M2M gets ready for a trillion sensors *(continued)*

patible single-board computer (SBC) based on the 1-W AMD Geode GX 500 processor. The PPM-GX sports an Ethernet controller, four 16C550-compatible UARTs, and two USB ports.

The paper "Communicating Machines Are Triggering an Embedded Revolution," which Burckle coauthored with Steve Pazol, president of nPhase, provides details on the emerging M2M market and on the variety of communications-link choices designers have. The authors differentiate M2M from more traditional industrial-control networks like SCADA (supervisory control and data acquisition) that impose restrictive, real-time requirements. M2M networks, they write, impose no such restrictions because they don't control processes; they "simply gather and pass along data to a central server." Because M2M networks don't depend on time-critical data and are therefore tolerant of network delays, the authors write, M2M-connected devices can be distributed across a wide area.

See the online version of this article (www.tmworld.com/2007_06) for a link to the complete paper, which provides additional information on how to choose from among the various wired and wireless communications options for your M2M networks.

Rick Nelson, Chief Editor

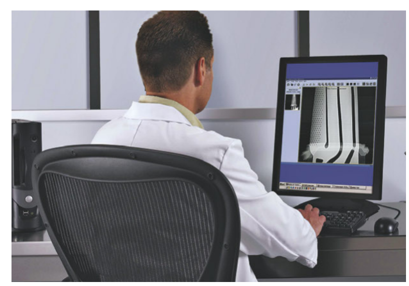
AEROSPACE TEST

Examining x-ray testing for aerospace

When used to inspect aerospace structures, x-ray inspection plays an important role in safety, quality assurance, and cost. The flaw-resolving capabilities of x-ray systems can mean the difference between life and death. Using x-ray systems, inspectors can examine areas of aerospace structures that would otherwise be uninspectable without dismantling them to gain access. Further, x-ray systems can inspect and detect damage that is too small to be discovered visually during "walk-around" checks.

"The success of space missions depends upon reliable parts," said Gary Stupian, scientist at The Aerospace Corp. "X-ray inspection is used both in the production screening of some types of components and as part of the investigation that ensues whenever a failure is encountered during ground testing."

X-ray inspection methods for aerospace and aircraft include film exposure, real-time imaging, imaging with digital detectors, and computed tomography (CT). Digital x-ray imaging techniques have been developed to a point where the resulting images are often of higher quality than those produced with traditional film radiography. "The cross-sectional image provided by 3-D x-ray computed-tomography techniques allows highly accurate measurement of even the thinnest geometries," commented Jason Robbins, director of operations at YXLON International.



A typical x-ray inspection process, such as investigation of this 2-D CT slice of a turbine blade, involves interpretation of results by a skilled individual. Courtesy of YXLON International.

Some very large x-ray machines have been built to accommodate the test requirements of aerospace parts like wings and engines. But portable systems are available for inspecting large structures that cannot conveniently be disassembled. Collecting x-ray images to test for features such as small cracks in very large structures will obviously result in a lot of data that must be reviewed.

See the online version of this article (www.tmworld.com/2007_06) for details on the inspection of turbine blades, ducts, air channels, and hydraulic lines.

Greg Reed, Contributing Technical Editor

PROJECTPROFILE

MODULAR INSTRUMENTS

So many combinations: Testing a switch-matrix board

DEVICE UNDER TEST

A switch-matrix board that routes any of eight programmable voltage signals to any of 96 output pins. The board generates digital patterns up to 20 MHz and 30 kV and has 36 Mbytes of memory. Four field-programmable gate arrays (FPGAs) generate the patterns, control 842 relays in the switch matrix, and communicate with the main controller.

THE CHALLENGE

Perform an automated functional test of power routing and memory. Measure DC voltage at each pin with a DMM and pulsed-power waveforms with an oscilloscope. Test all memory locations. Automatically connect a DMM and an oscilloscope to any pin under software control. Design a text fixture that allows for easy removal of the board under test.

THE TOOLS

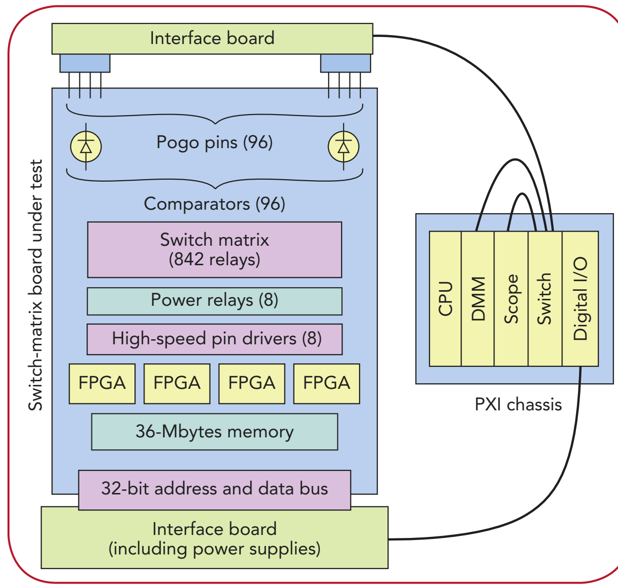
- A&F Fixture Products: reverse bed-of-nails fixture. www.affp.com.
- Boston Engineering: custom interface PCB that connects the PXI instruments to the unit under test. www.boston-engineering.com.
- National Instruments: PXI chassis, DMM, oscilloscope, switching cards, digital I/O cards, graphical programming language. www.ni.com.

PROJECT DESCRIPTION

Boston Engineering (www.boston-engineering.com) designed a switch-matrix board for use in an electrostatic-discharge (ESD) tester. The board routes signals from eight power supplies to 96 output pins. Senior controls engineer Eric Atherton developed an automated functional tester that reduced test time from 1 to 5 days to less than 1 hr while testing all power supply and pin combinations.

Prior to development of the automated tester, a technician would program each board under test by entering codes to the memory through a command-line interface. All connections to the board were performed manually.

With Atherton's automated tester, the switch-matrix board under test routes any of the eight power supplies (0.7 VDC to 15 VDC) to any of the 96 pins located along the edge of the board. That's 96^8 possible combinations. The board's 36 Mbytes of memory store sequencing data for all pogo pins.



An automated tester exercises and measures signals from a switch-matrix board.

The tester's high-frequency interface board includes the power supplies, and the board routes data from four PXI digital I/O cards to the board under test. The digital I/O cards can load and read data from the switch-matrix board's memory, and they can control the relays on the switch-matrix board during a test.

Testing starts with signal routing. The interface board puts the test system in direct control of the switch-matrix board's switching capabilities. The first test involves switching each of the eight power supplies to each of the 96 pogo pins. The PXI DMM card measures the DC voltage at each pin, with signals routed through four 24-channel PXI switching cards. The software compares each measurement to specified limits.

Next, the digital I/O cards control the pin drivers at 20 Msamples/s, which produces a 10-MHz pulsed output at each pogo pin. The PXI switch cards then connect the oscilloscope to the pogo pins where the system captures each 10-MHz signal.

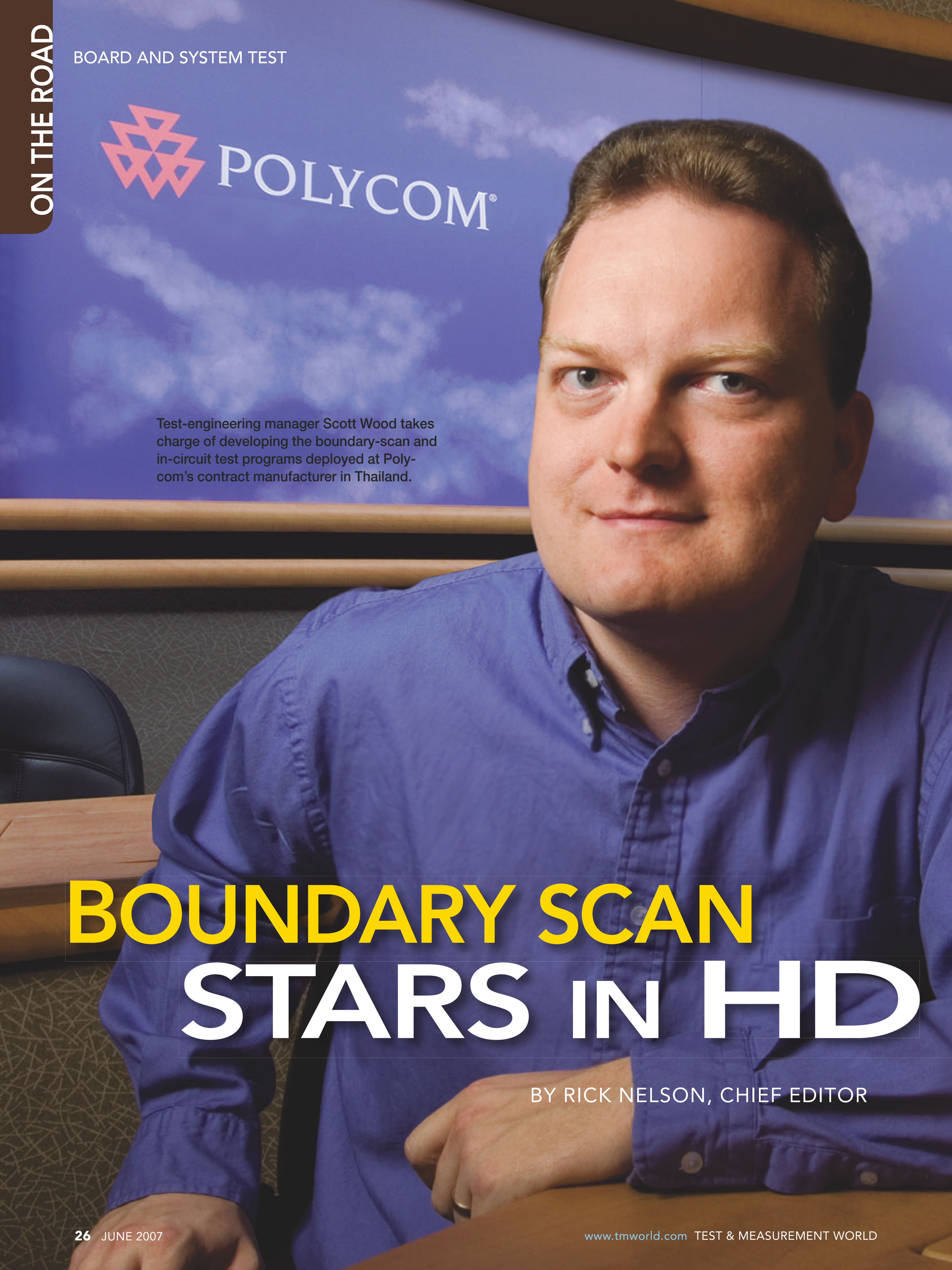
For the memory test, PXI digital I/O cards load the board's 36 Mbytes of memory with alternating bit patterns (55 hex and AA hex). The cards then read back the data from memory.

Next, the tester exercises the FPGAs to verify that they properly control signal routing. The FPGAs decode data from the memory into control signals for the board's relays, switch matrix, and pin drivers. The DMM and oscilloscope measure the output signals at each pin.

LESSONS LEARNED

Reliable mechanical figures are an important part of any test system. Many test fixtures use pogo pins to connect test equipment to a board under test. In this case, the pins were located on the edge of and parallel with the board under test, extruding over the edge. Boston Engineering designed an interface board with connectors that mated to the board under test. The reverse bed-of-nails fixture holds the board in place while a mechanical lever raises and lowered the connector board, mating to the pogo pins.

Martin Rowe, Senior Technical Editor



Test-engineering manager Scott Wood takes charge of developing the boundary-scan and in-circuit test programs deployed at Polycom's contract manufacturer in Thailand.

BOUNDARY SCAN STARS IN HD

BY RICK NELSON, CHIEF EDITOR

DAN BRYANT

AUSTIN, TX. Videoconferencing promises to revolutionize interpersonal communication in myriad applications. Although the concept is not new, recent advances are extending the technology well beyond the talking-heads format of formal business meetings. The audio and video qualities as well as the ability to track motion have become sufficiently sophisticated to open up new applications in real estate, manufacturing, medicine, and education.

One manufacturer that is devoted to expanding the capabilities of videoconferencing is Polycom. Here are just a few applications that were made possible by Polycom's new generation of HDX high-definition videoconferencing systems, which the company introduced last November:

- The Cleveland Museum of Art uses videoconferencing to make art and artifacts available outside the museum, to develop programs in conjunction with teachers across the US, and to teach a distance-learning three-credit semester-length university-level art course.
- Mote Marine Laboratory uses Polycom systems to present live, interactive distance-learning programs to students of all ages; the organization uses videoconferencing to project its 135,000-gallon shark tank in Sarasota, FL, to such far-flung locations as Fargo, ND.

CONFERENCING

Engineers at Polycom chose IEEE 1149.1 JTAG technology to ensure the testability of their company's new high-definition videoconferencing system.

- The Beth Melsky agency uses Polycom equipment to stage remote casting calls, allowing a director in Los Angeles, for instance, to audition an actor in New York.

ICT becomes insufficient

But when engineers at Polycom embarked on their development process for the new high-definition (HD) systems, they realized they would face some tough challenges. For example, when they began auditioning components for the systems, and when they began designing printed-circuit-board (PCB) stages on which these components would play, they knew their existing in-circuit test (ICT) strategy would no longer suffice.

Scott Wood, test-engineering manager, explained, "It was clear that chips and components and circuitry necessary to produce the high-definition video inputs and outputs would require very dense multilayer boards—there are probably five times as many components in our new product than were in the most complicated of our older products. So because of board complexity, it was clear that our traditional ICT wasn't going to work if we wanted to maintain the test coverage that we've had historically."

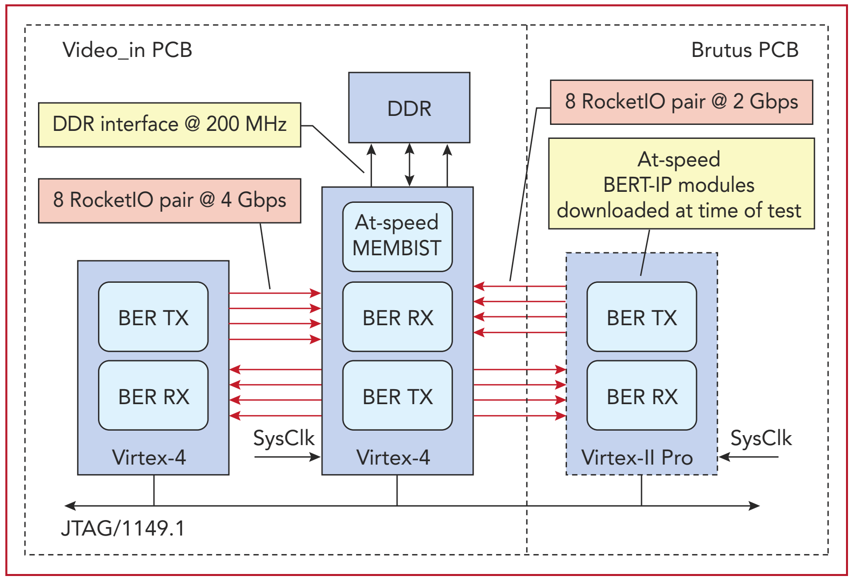
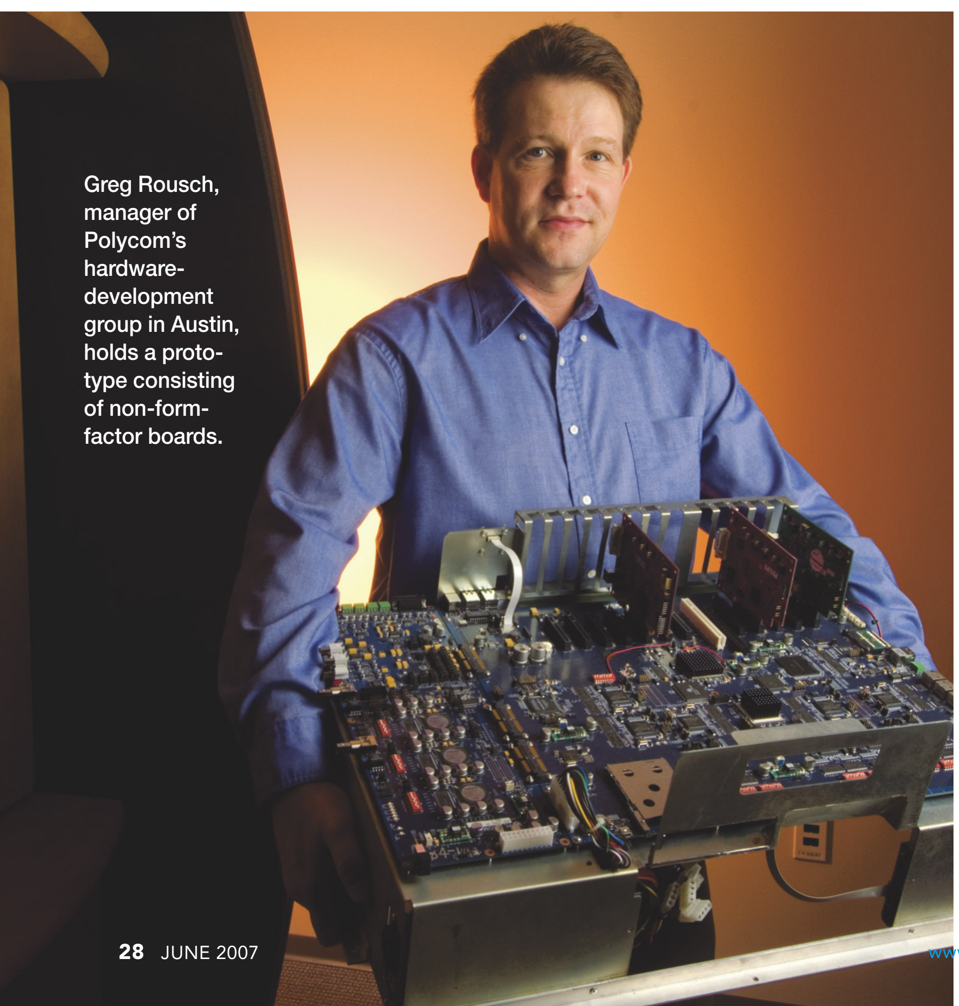


FIGURE 1. Intellitech's BERT-IP modules take the form of downloadable bit streams that configure built-in test structures within the Xilinx Virtex-II Pro and Virtex-4 FPGAs used on the Polycom boards.

DAN BRYANT



Greg Rousch, manager of Polycom's hardware-development group in Austin, holds a prototype consisting of non-form-factor boards.

Chief among the challenges would be the presence of high-density micro ball-grid arrays (BGAs) and other high-density solder-ball chips, as the bed-of-nails fixtures used on earlier-generation products could not provide the necessary levels of test coverage for these components. The engineers knew that they needed an alternative technology. Further, the difficulties would present themselves not just during high-volume production but also during development: Polycom's hardware engineers needed to supply their software-engineering counterparts with sufficient hardware prototypes to exercise the code under development.

Walter Haskell, senior staff engineer at Polycom, said that the HD system development began with what he and his colleagues call a "non-form-factor" board—one that's larger than the production boards ultimately used in the new system but, nevertheless, one designed to embody the new system's functionality. "Because of the complexity—we have so many processors and signals—the law of averages said that if we didn't have some good way of checking things out, we would be plagued with problems."

His recommendation? "I started thinking of boundary scan as an option."

Greg Rousch, manager of the hardware-development group, concurred. "Boundary scan has been out there for almost my whole career, but I had never

used it until we began this development effort. Up until then, we had just always used bed-of-nails test fixtures. Our layout team put dedicated test points down to support bed-of-nails ICT test fixturing, and that's just always been good enough. What has changed that are the high-density ball-grid-array packages, because it's very difficult to probe on a board and measure the soldering quality of a BGA package."

Rousch added that not only are board densities getting to the point where it's hard to place test points, but that even if board real estate is available, putting test points on high-speed nets can adversely affect signal integrity. Taking such factors into consideration, he explained, "When Walter came to me and said that he really felt we should be considering boundary scan for this product, I agreed."

Wood noted that Polycom continues to employ ICT for mixed-signal and other device test that's not amenable to boundary-scan, but he added that the Intellitech boundary-scan implementation Polycom chose—the Eclipse system—can test most of the digital portions of the boards, including high-speed RocketIO

Senior staff engineer Walter Haskell concluded that boundary scan would be the best option for testing the many processors and signals on Polycom's new high-definition videoconferencing systems.

DAN BRYANT

data lines carrying HD video signals at rates to 4 Gbps between field-programmable gate arrays (FPGAs) (**Figure 1**).

Intellitech's RocketIO test capability is based on an at-speed BERT-IP test module that works in conjunction with Intellitech's Eclipse JTAG system. The BERT-IP module takes the form of a downloadable bit stream that configures built-in test structures within the Xilinx Virtex-II Pro and Virtex-4 FPGAs used on the Polycom boards. The configured built-in test structures include pattern generators, high-speed transceiver controls, and pattern receivers that enable the real-time detection and display of bit errors.

The Intellitech at-speed test function also enables indirect test of parameters such as clock oscillator jitter and DC/DC-converter noise as well as voltage levels that are not testable using standard JTAG capabilities. In addition, it can test DDR and RocketIO termination resistors, DC blocking capacitors on RocketIO differential lines, and the RocketIO lines themselves that don't include 1149.1 boundary-scan cells.

But for the regular analog components, Wood said, the team continues to rely on ICT. "Boundary-scan coverage gets us almost all the way there and allows us to do things that with ICT alone wouldn't be possible. But for those areas that boundary scan can't cover, we use a much more limited ICT fixture than we used to use to get near 100% coverage." *(continued)*

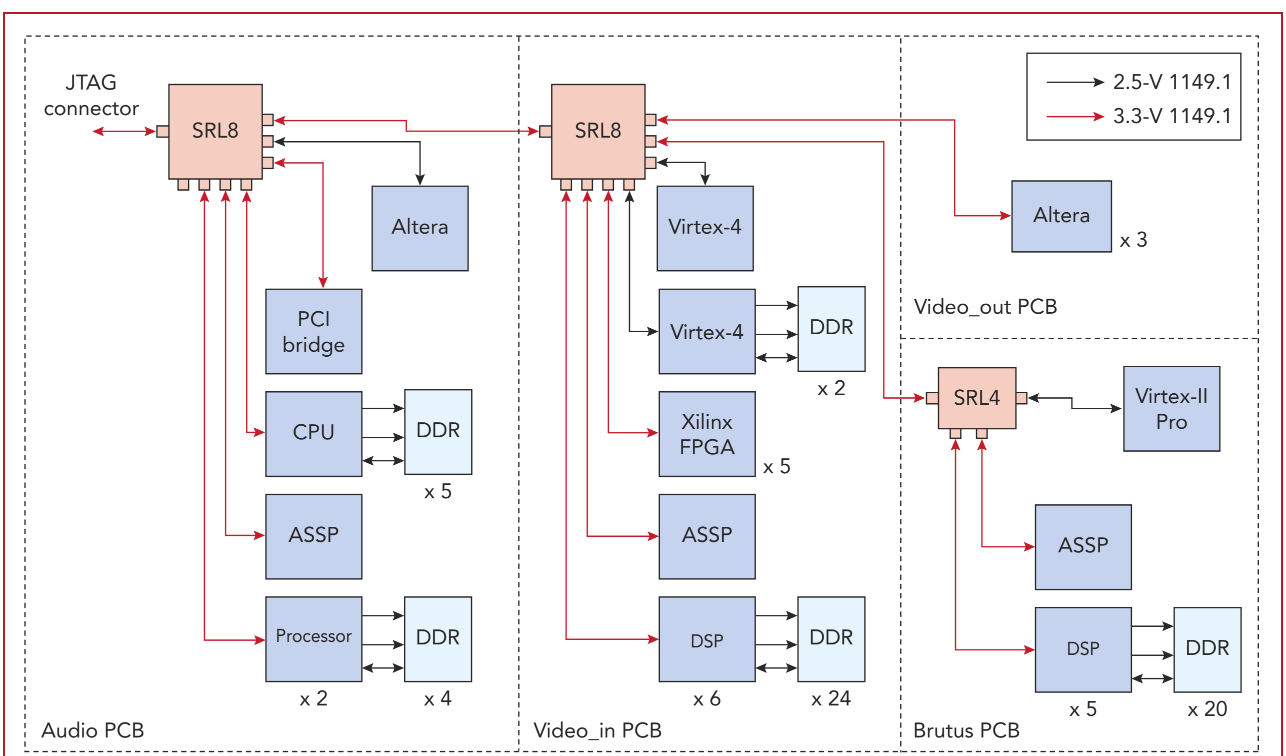


FIGURE 2. A Scan Ring Linker (SRL) on each board serves as a high-speed JTAG test-bus interface, linking secondary scan chains to a single IEEE 1149.1 external interface. A single JTAG connector enables multiboard test.

Simplifying boundary-scan I/O

In addition to the Eclipse system and BERT-IP, the Polycom team also made use of Intellitech's Scan Ring Linker (SRL)—a high-speed JTAG test-bus interface. The SRL links secondary scan chains into a single high-speed test bus connected to a single IEEE 1149.1 external interface.

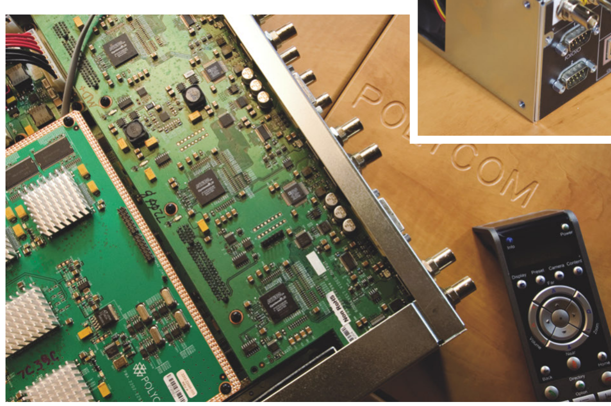
"Instead of having 10 or 15 different external scan-chain connectors and cables," said Wood, "the SRL lets us use one connector and cable per board to make our boundary-scan connections." The SRL also permits a single connector to enable multiboard tests, and it supports multiple voltage domains, as shown in **Figure 2**.

Wood said that in the future, he intends to take advantage of Eclipse's links to National Instruments' LabView—the program he has traditionally used to develop his manufacturing test programs. "Intellitech has a nice LabView interface to its boundary-scan software. We haven't implemented that yet, but when we do, it will further simplify our test deployment to our contract manufacturer."

When asked whether he had difficulty convincing his contract manufacturer's (CM's) engineers to employ boundary scan, Wood said, "The bottom line was when they saw the complexity of this product relative to the other products they had built, it was obvious to them, especially from a debugging perspective, that boundary scan was going to be invaluable. It was immediately obvious to them that this was the only way they were going to get access, so there wasn't any pushback. It saves them a lot of time, which is what they are most interested in—they need to be able to get high-quality products out the door that work. And when they don't work, they need to be able to quickly identify problems and fix them. Boundary scan helps them do that."

The Polycom engineers try to focus on design, shifting test responsibilities onto its CM. Speaking of the CM engineers, Wood said, "We have been working with this group for so long that we have a great working relationship with them." Rousch seconded that: "They are very competent test engineers—in fact, two of them, who are Thai citizens, trained at UT Austin. When we completed our test program, Scott literally just made a copy of it and went over to Thailand and set it up."

Nevertheless, said Wood, although the CM test engineers "can handle most ICT-related problems without having to get us involved too often, we are still in the beginning stage of using boundary scan, so they are still dependent on us to help resolve some issues they come across. But as more and more of our products start to use boundary scan, we will push more of the responsibility back on to them."



DAN BRYANT

The many I/O channels (top) and the circuit-board density (bottom) of Polycom's HDX videoconferencing system made it necessary for the product's development team to augment in-circuit test with boundary scan.

Boundary scan in prototypes

Wood's primary responsibility is production test, but boundary scan has been important to the Polycom team from initial prototype stages. Said Rousch, "We tried as hard as we could to have the boundary-scan test available on our very first prototype, which was a massive non-form-factor board."

Because boundary scan was new to the Polycom team, they delegated boundary-scan program development to Intellitech, providing Electronic Design Interchange Format (EDIF) netlists as input. Fortunately, said Rousch, "Intellitech did a good job of keeping up with us as far as having tests ready. As soon as our first board came off the assembly line here at a local assembly shop, [Intellitech applications engineer] Carl Nielsen flew down here and almost in real time was debugging his program and also finding bugs in our product at the very same time. It was a big help right during that first bring-up to use boundary scan as a design debug tool."

Asked about additional test challenges he faces, Rousch said, "My team develops all the board-level hardware for our products, but we have a whole floor of software engineers. Most of the magic is in the software, so we are critically dependent on the software team. My biggest test challenge is that the software team is running behind the hardware team, and we really need the software to fully exercise our hardware."

Haskell, the senior staff engineer, proposed a possible boundary-scan solution to this problem: "We would like to go further with boundary scan to where we can manually toggle some pins on a prototype board. In some instances we might think a pin should be in a certain state, but it's not—possibly because of software issues. If we could use boundary scan to toggle those pins, we could speed up our hardware debug while waiting for software updates."

Rousch noted that there is a flip side to the problem of hardware teams waiting on software: "Because there are so many software developers, we get a tremendous amount of pressure to make lots of copies of prototypes even before We've had a chance to completely debug them." Ideally, he said, the software engineers would be able to simulate their software running on the target hardware without actually having the target hardware available. "That's an old problem that's been around ever since I've been in the industry. If hardware technology

stayed static, the industry could catch up. But the hardware just keeps getting more and more complex. The modeling technology always lags, and for video designs, it never catches up."

In fact, Rousch said, in this respect, the industry has lost ground. "In the late '80s and early '90s, I worked for a medical equipment company, and we used to model complete boards—the chips were smaller, and there was a whole industry set up for supplying models for co-simulation environments. The simulations would run really slowly, but at least they would run. But in the last 10 or 15 years, everyone just gave up. The chips got bigger and more complex, and good models often weren't available, so board simulation fell apart. The only place we do simulation now is with FPGAs."

In addition to an effective co-simulation environment, Rousch has another item on his test wish list: "In general, digital video is very difficult to test. It takes an enormous amount of test vectors to really test digital video. If something could be done to give better coverage with less test time, we would always be looking for some innovation there."

Wood has his own wish list. In terms of OS support, he said, he would like to move away from Windows toward an open-source system. "As a rule in our organization, we use open-source software wherever possible." Most of Polycom's production line, he added, runs off Linux.

But the team is nevertheless satisfied with its initial boundary-scan experiences. Said Rousch, "We are absolutely going to continue using boundary scan." Added Wood, "Our first HDX product design was a huge leap. As we continue developing new products on an ever more accelerated cycle, we will be looking at ways to apply boundary scan even more effectively." T&MW

FOR FURTHER READING

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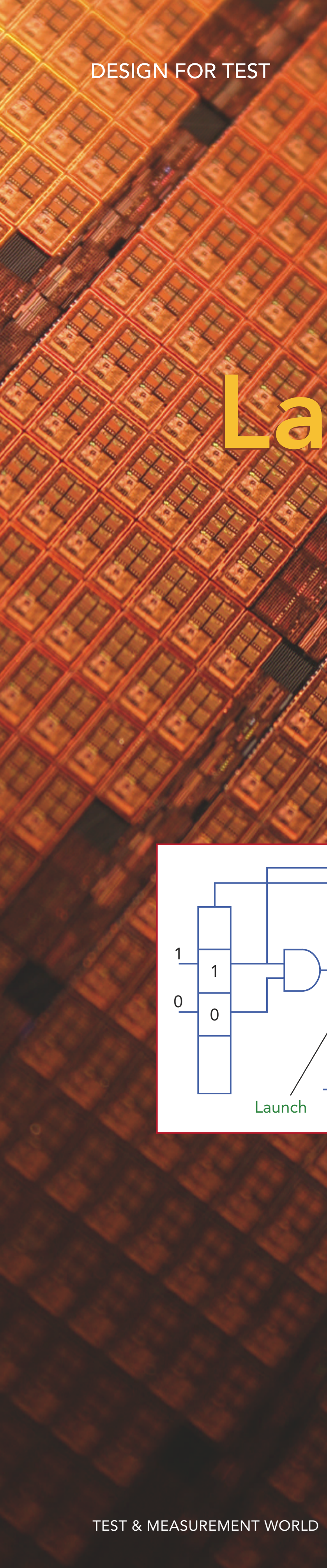


A comparison of broadside-transition-pattern and launch-off-shift techniques shows the latter to be viable for testing a 90-nm wireless baseband device.

Launch-off-shift AT-SPEED TEST

BY NOAM BENAYAHU AND ARIK CHECHIK, METALINK, AND RON PRESS, MENTOR GRAPHICS

Both launch-off-shift (LOS) and broadside-transition-pattern techniques are finding use in the at-speed test of devices fabricated in 130-nm processes and below. The broadside-transition-pattern approach is most commonly used, but our experiments in applying both techniques to the test of a wireless baseband device show that LOS can provide advantages.

At-speed scan test serves applications for which static testing is not sufficient (Ref. 1). The basic operation of at-speed scan testing involves loading the scan chains at a slow clock rate and then applying two clock pulses at the functional frequency (**Figure 1**). The first pulse causes a transition to start propagating from a scan-cell. The second pulse captures the scan cell value at the end of the path being tested.

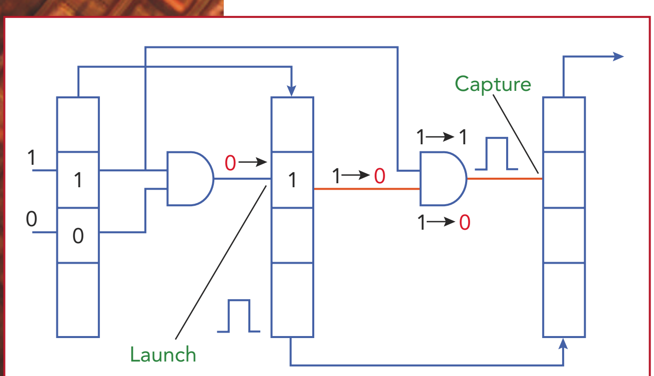


FIGURE 1. At-speed scan test involves loading scan chains at a slow clock rate and then applying two clock pulses at the functional frequency.

If the circuit is operational, then the transition will propagate to the end of the path in time and the correct value will be captured. Otherwise, if a delay causes a slow propagation, the transition from launch to capture cell will be slow, an erroneous value will be captured, and the defect will be detected.

The most popular at-speed scan pattern is the transition pattern (Ref. 2). A potential fault of slow to rise (0 to 1) and slow to fall (1 to 0) is modeled at every gate terminal within the design. Automatic test-program generation (ATPG) tools target these fault sites and cause a transition using any launch scan cell and capture results using any downstream scan cell.

Using PLLs for accurate clocks

A fundamental problem with at-speed scan testing is how to apply accurate clocking for the at-speed launch and capture pulses. Traditional stuck-at scan patterns are static. Stuck-at clocking for loading the scan chain and capturing results is often performed at frequencies between 10 MHz and 40 MHz. At-speed scan testing can load the scan chains with a clock frequency that is similar to the one used for stuck-at tests, but the launch and capture pulses must be applied at the functional frequency.

Supplying the at-speed clock for launch and capture from a tester becomes more demanding as the desired frequency increases. A solution of using some basic programmability around device internal phase-locked loops (PLLs) provides a nice option (Ref. 3). Providing internal PLL control for at-speed test has become a common practice for at-speed scan testing (Refs. 4 and 5).

The most common technique for applying at-speed transition patterns is referred to as a broadside or launch-from-capture pattern type (Ref. 6), as shown in **Figure 2**. With this pattern type, the scan chain is loaded and then placed in functional/capture mode by forcing scan_enable (SE) to 0. Sometimes, an extra cycle is added to the test pattern that has no activity to ensure that the scan_enable completely settles. Next, two pulses are generated to launch and capture the transition.

The broadside pattern launches the transition in the functional mode of operation, so it is likely to propagate transitions along paths that are real functional paths. Often, the coverage report from broadside pattern ATPG can be 10% lower than standard static stuck-at patterns.

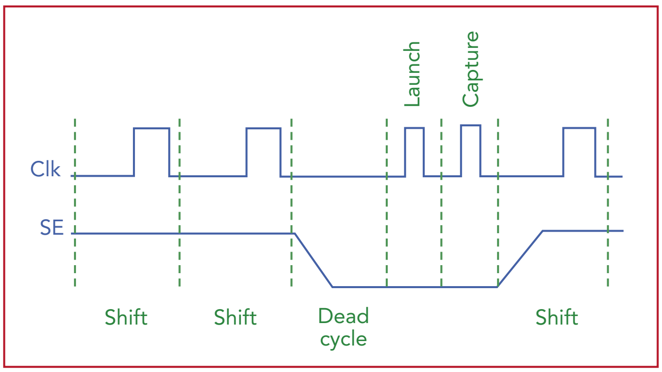


FIGURE 2. With broadside transition patterns, a scan chain is loaded and then placed in functional/capture mode by forcing scan_enable (SE) to 0.

Launch-off-shift patterns

With LOS patterns (**Figure 3**), the launch occurs during the last shift while loading the scan chain. Next, the circuit is placed into functional/capture mode very quickly so an at-speed functional clock can be pulsed.

ATPG is much easier with LOS compared to broadside patterns. It is a simple ATPG activity to load the starting value for a transition directly to the scan cell one shift before the last and then load the transition value in the last shift. Broadside patterns require ATPG to calculate the transition value through the combinational logic, since it is in functional mode during the launch pulse. In addition, LOS patterns usually report higher coverage than broadside patterns.

LOS reports higher coverage and is easier for ATPG, so it results in fewer patterns and faster ATPG run times compared to broadside patterns. So, why is broadside transition test more popular than LOS patterns?

There are two primary reasons for the reluctance to use LOS patterns. The first is the difficulty to make the circuit change from shift mode to functional/capture mode between the last shift and functional clock pulse. If standard scan_enable architecture is used, then the scan_enable must be routed as a clock. Furthermore, since scan_enable goes to all sequential elements, it is a global clock and must settle at the system clock frequency. One way to work around this issue is to add pipelining logic throughout the device for scan_enable (Ref. 7).

Pipelining scan_enable adds additional test logic to the design, but it removes the difficult task of treating scan_enable as a global clock. As shown in **Figure 4**, the clock triggers a change within the local scan_enable.

The other common concern with LOS patterns is that they may test the circuit through paths that are not possible functionally. LOS patterns can shift in a transition that is impossible during normal circuit operation.

An important question to ask is how much of the additional coverage beyond broadside patterns is due to nonfunctional logic? It's possible that testing nonfunctional logic during at-speed tests will falsely report failures and result in yield loss (Ref. 8).

(continued)

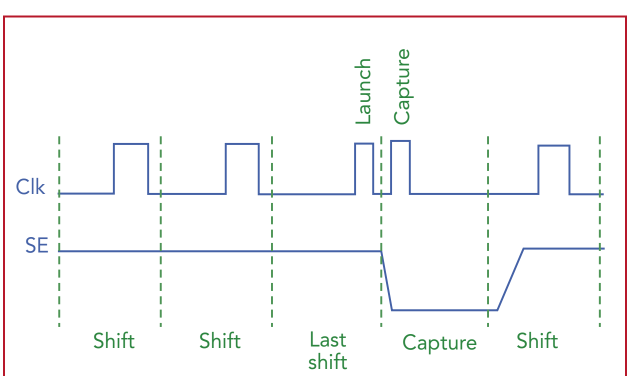


FIGURE 3. In a launch-off-shift transition pattern, the launch occurs during the last shift while loading the scan chain.

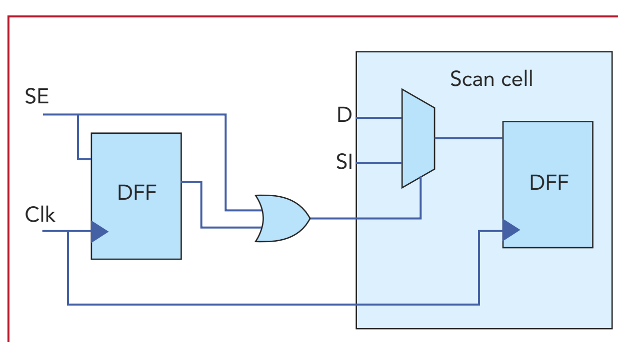
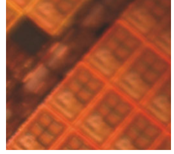


FIGURE 4. Pipelining scan_enable adds additional test logic to the design, but it removes the difficult task of treating scan_enable like a global clock.



Accounting for false and multicycle paths

During the design process, many paths are determined to be either false or multicycle paths. A standard Synopsys Design Constraints (SDC) file lists false and multicycle paths such that special efforts are not made for timing closure at these paths. Two types of false paths can exist. Some false paths cannot be sensitized and are not possible during functional operation (but may be possible during scan mode). The other types of false paths are paths that are not intended to operate at system frequencies. Multicycle paths require more than one functional clock cycle to propagate.

Both false and multicycle paths must be considered during at-speed scan testing. Scan has the potential to directly load scan cells into a circuit state that isn't possible during functional operation. As a result, false or multicycle paths may be activated during at-speed scan testing. If the at-speed scan tests fail due to these paths, then correctly functioning devices may be falsely discarded. The result could be yield loss.

To avoid such loss, engineers have often tested for false and multicycle paths during time-based simulation and test program tester integration, and they have often performed these tasks manually.

Fortunately, automation has been added to ATPG tools so they can now directly read standard SDC files and extract the timing-exception path information (Ref. 9). With this automation, if a test propagates a signal along a false or multicycle path that is sensitized during ATPG, then the capture scan cell will capture an unknown X value.

Baseband-chip case study

Metalink, a company that designs wireless and wireline broadband communication chips, needed to develop an effective test strategy for its WLANPlus 802.11n-draft-compliant wireless LAN technology, which is optimized for the networked home entertainment environment. The company's WLANPlus family consists of the MtW8171 baseband device and the MtW8151 RFIC. The MtW8171 baseband chip is manufactured at a 90-nm low-power process and implements full at-speed scan-test capability. For this device, at-speed scan was implemented using both LOS and broadside transition patterns.

To reduce the increased pattern count required to cover transition faults, we implemented compression logic using Mentor Graphics Embedded Deterministic Test technology. The bring-up of the scan program for this chip took only two days from the chip arrival to the moment where all bring-up patterns were up and running at-speed.

We performed experiments to compare the difference between broadside and LOS coverage. We generated the initial patterns by using procedures that define specific clock sequences that can be used.

Table 1. Comparison of broadside and launch-off-shift

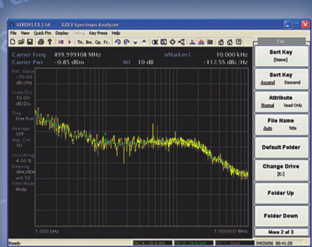
	Broadside	Launch-off-shift
Initial coverage	71.38%	78.57%
With SDC	69.55%	72.88%

Table 1 shows the results of transition pattern generation. Initially, the LOS patterns reported 78.57% test coverage compared to 71.38% for broadside patterns. Thus, LOS appeared to test >7% more faults. Next, we considered false and multicycle paths, since these paths are not intended to operate at functional clock rates.

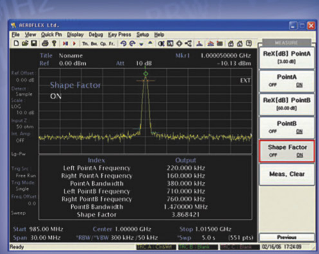
After accounting for false and multicycle paths (MCPs), the LOS and broadside coverages were reduced to 72.88% and 69.55%, respectively. Therefore, 5.69% of faults reported in the initial LOS detection were false paths and MCPs. Similarly, 1.83% of broadside detection was due to false paths and MCPs. Based on these results, we concluded that a significant portion of the advantage in test coverage with LOS patterns are due to false-path and MCP testing.

These results imply that when effective false and multicycle paths are considered for LOS patterns, the risk of overtesting is reduced. As a result, LOS can be an attractive ATPG approach for at-speed test. Pattern-generation time and pattern count can be significantly smaller than broadside patterns with similar coverage. The combination of pipelined scan_enable and false and multicycle path consideration solve the most common concerns with LOS patterns. Broadside

Performance far beyond the price tag



Phase noise



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patterns should still be used to top-off coverage since LOS patterns will be unable to detect some faults.

What's next?

Manufacturers are continuing to look for ways to improve the effectiveness of at-speed scan testing. One approach, referred to as "timing-aware" ATPG (Ref. 10), targets small delay defects. It attempts to test each fault by propagating the transition down as slow a path (smallest slack) as possible. In this technique, the at-speed test pattern set is more likely to detect small defects that could escape a normal transition test set.

Another new approach to at-speed scan testing is to apply a series of at-speed shifts just before the launch cycle. Such "BurstMode" ATPG (Ref. 11) helps the at-speed clock pulses behave more like functional frequency pulses. It lessens the drooping of the voltage supply caused by the sudden pulsing of at-speed clocks for launch and capture during normal transition tests. False and multicycle path handling should be considered with both of these techniques to avoid the risk overtesting.

Manufacturers continue to look for ways to improve the effectiveness of at-speed scan testing.

Meanwhile, techniques such as pipelined scan_enable make LOS more feasible, allowing users to evaluate the trade-offs between the two transition pattern types and determine which is the best solution for them. Broadside patterns offer less logic insertion and less nonfunctional path tests, while LOS patterns offer faster pattern generation and fewer patterns. The LOS approach may also be desirable for companies that are interested in detecting any type of defect, including those that are nonfunctional. Fortunately, the common concern with overtesting can be alleviated by ATPG tool handling of false and multicycle paths through SDC files that are common in design flows. T&MW

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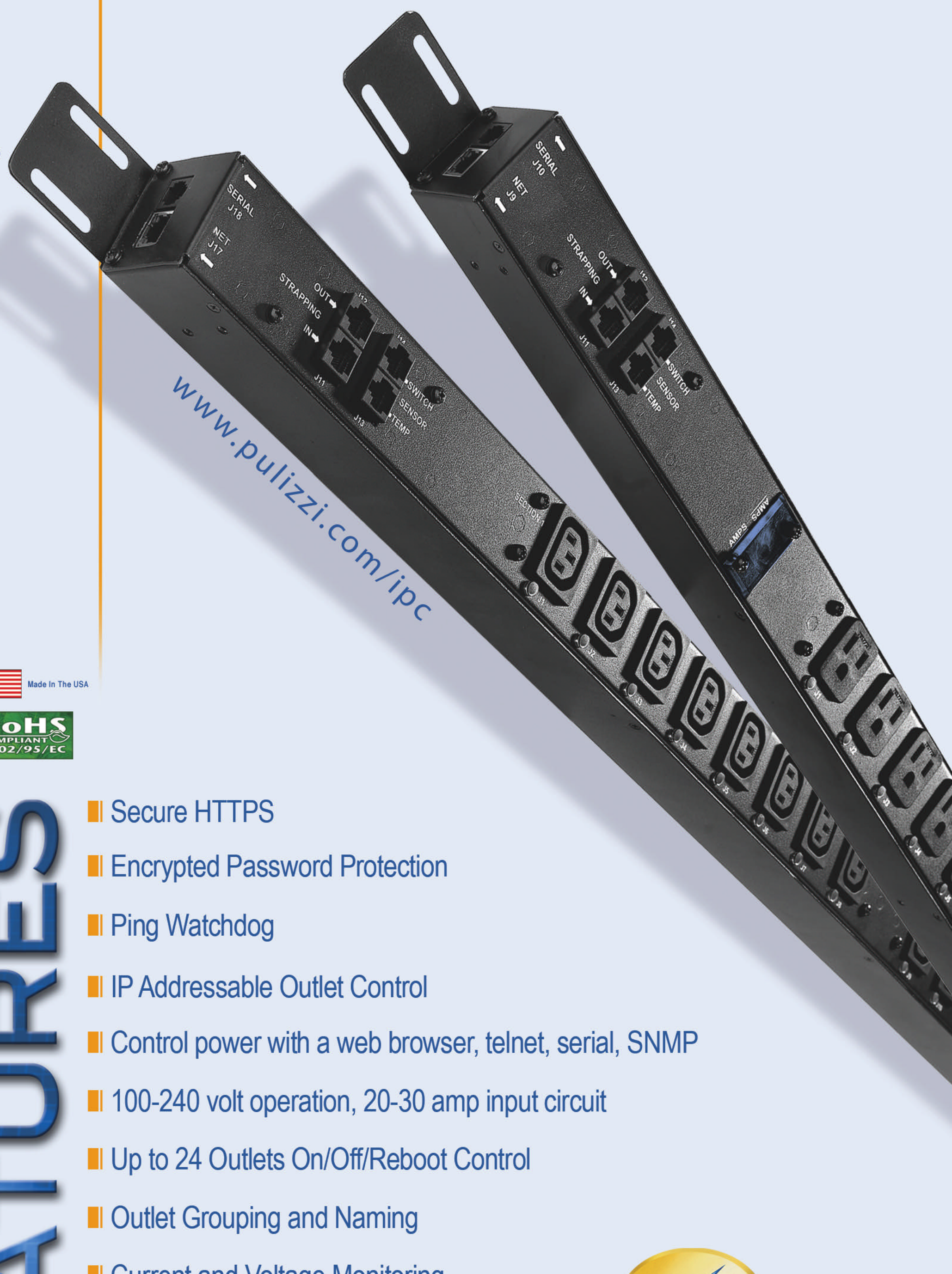

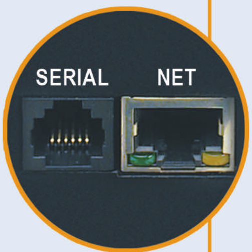

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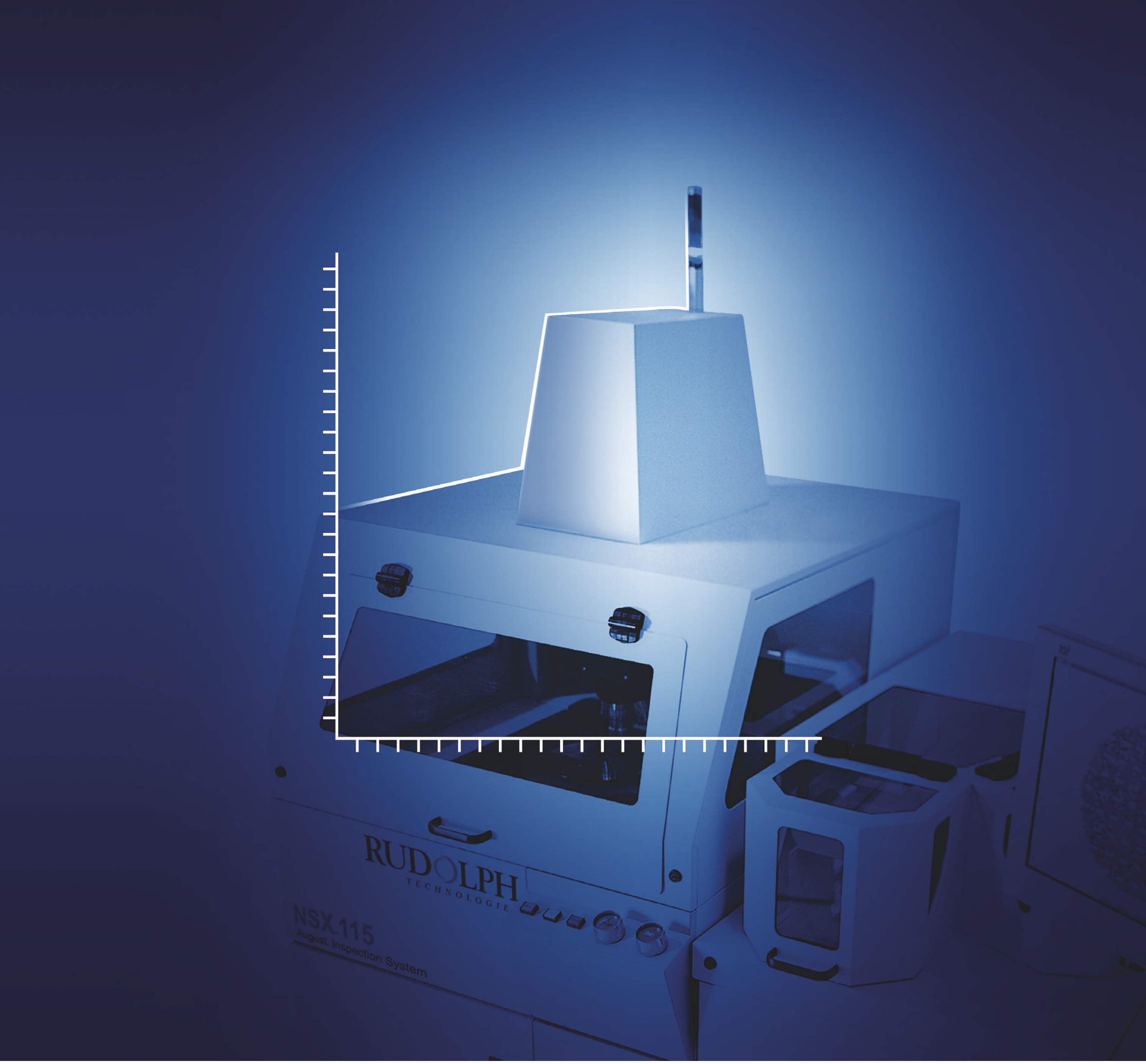

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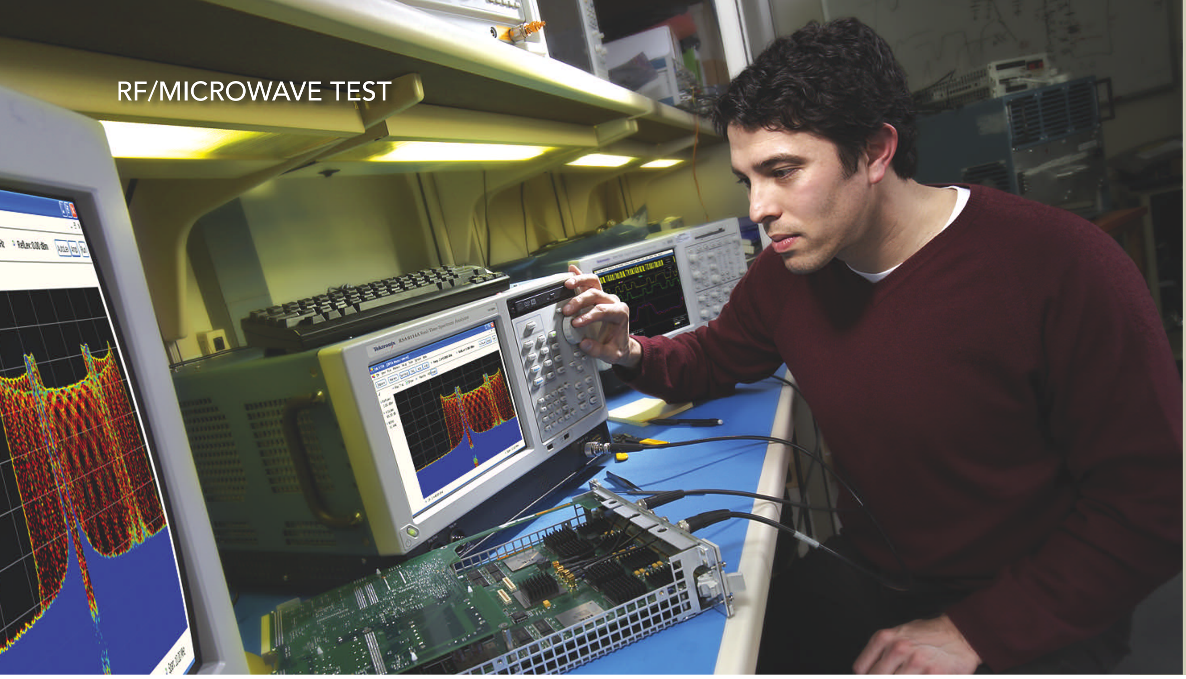


The DPX spectrum display on the Tektronix RSA6100A spectrum analyzer offers a live color view of signal transients in the frequency domain, and the color indicates how often the transients have occurred.
Courtesy of Tektronix.

SPECTRUM ANALYZERS *respond to* DIGITAL MODULATION

Digital RF techniques such as W-CDMA and WiMAX require measurements that classic swept-spectrum analyzers can't handle.

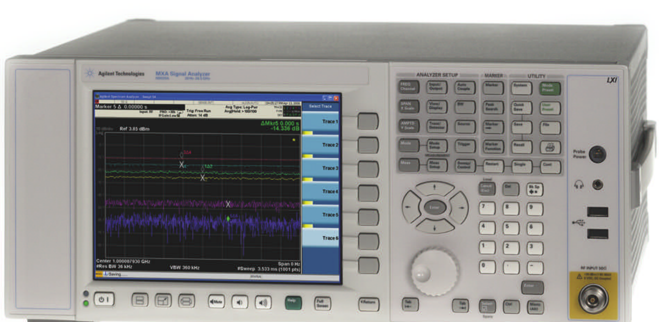
BY PAUL G. SCHREIER, CONTRIBUTING TECHNICAL EDITOR

We all love our wireless devices. We want more features, higher data rates, and improved range. These demands, in turn, require advanced digital protocols. Meanwhile, the number of signal sources is increasing dramatically, and interference is getting worse.

Engineers need test tools that can help them implement advanced protocols in the lab and the field. Fortunately, the necessary test instruments—whether you call them signal analyzers or spectrum analyzers—are increasing their capabilities to keep pace with these developments. The online version of this article includes a chart listing 2.5-GHz and up spectrum analyzers (www.tmworld.com/2007_06).

"Innovation in radio technology is exploding," explained Elaine May, director of marketing for the real-time spectrum analyzer product line at Tektronix. "What radios previously did in the analog domain, they're now doing in the digital domain. This adoption of digital technology also means that they now benefit from the instrument version of Moore's Law: In the past, more performance meant a higher price, but today's instruments are not only getting more powerful, they're getting less expensive."

An important trend, agreed almost all manufacturers of spectrum analyzers, is the move toward wider frequency ranges and wider capture bandwidths to accommodate new modulation schemes. Explained Mark Elo, director of business development for RF products at

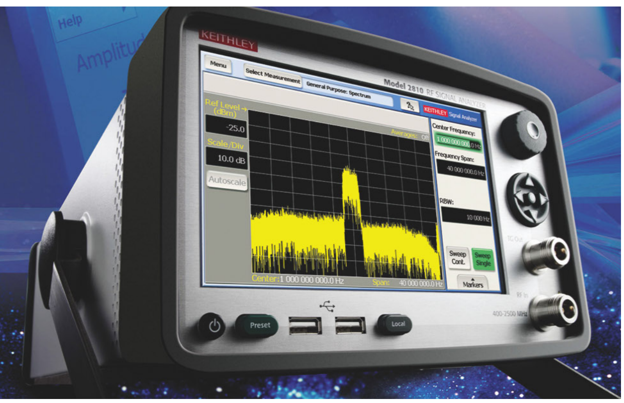


Agilent's MXA signal analyzer Model N9020A, with family members whose ranges go from 20 Hz to either 3.6, 8.4, 13.6, or 26.5 GHz, comes with built-in software for advanced modulation analysis and troubleshooting for schemes including WiMAX, UWB, 2G, 3G, 3.5G, WLAN, digital video, and 30 other formats. The MXA can simultaneously display multiple traces (6 max) and markers (12 max).
Courtesy of Agilent Technologies.

Keithley Instruments, "Ten years ago, GSM was popular and had a 300-kHz bandwidth. Then came W-CDMA with 5 MHz. Now, we've got WiMAX and multiple-input multiple-output [MIMO] systems with bandwidths as large as 40 MHz."

Instruments for modern requirements

For these more complex communications schemes, traditional swept-tuned spectrum analyzers can't demodulate signals.



The Model 2810 RF vector signal analyzer from Keithley accepts three user-installable analysis options for testing mobile-phone handsets based on either GSM/GPRS/EDGE, cdma2000, or W-CDMA. Courtesy of Keithley Instruments.

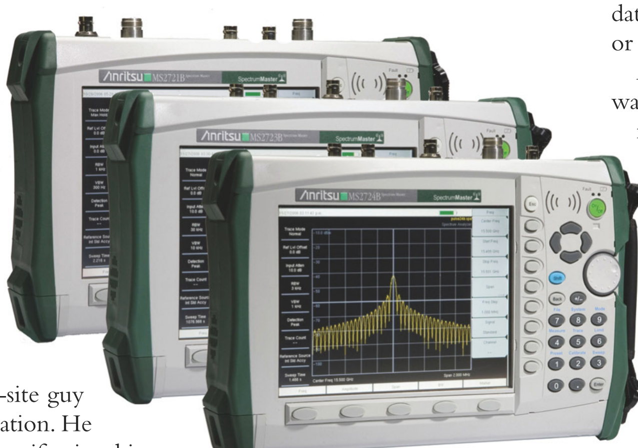
Based on a classic architecture from the 1940s, the analyzers use either a local oscillator or a digitally synthesized frequency source to sweep or step through a range of frequencies and then use filters to measure the signal power in particular segments. The results appear as a plot of amplitude vs. frequency.

Thus, in simplified terms, these analyzers are superheterodyne receivers with a display, but they still have an important role. Bryan Harber, product manager for microwave and spectrum analyzers at Aeroflex, commented, "The average cell-site guy isn't interested in demodulation. He wants a spectrum mask to see if a signal is within bounds." Added Herbert Schmitt, product manager for spectrum and network analyzers at Rohde & Schwarz, "The swept architecture has a brilliant future. There are tons of applications where users look for spurious signals, harmonics, and phase noise."

But because of the measurement tasks for which they were designed, these classic analyzers have a small capture bandwidth and can easily miss simultaneous signals, a rapid change, or a momentary pulse that falls outside that bandwidth. This is where a wide capture bandwidth, also called the resolution bandwidth (RBW), is useful along with demodulation information.

An instrument that offers these capabilities was initially called a signal analyzer and more recently a vector signal analyzer (VSA), but today many units called spectrum analyzers also offer this capability. Indeed, said Rohde & Schwarz's Schmitt, "The difference between spectrum analyzers and signal analyzers has become artificial. All modern spectrum analyzers have a digital back end and can do the tasks we previously associated with signal analysis. Even in midrange and some low-end units, you can find demodulation options for common standards."

A signal analyzer's front end looks like that of a swept analyzer, except it digitizes the signal for digital postprocessing. Signal analyzers also have a large RBW to capture a wideband signal and any digital modulation effects at one instant in time. Most models use an internal CPU to run built-in routines or optional firmware "personality packs" that demodulate a specific modulation scheme (such as GSM, 3GPP, TD-SCDMA, and WLAN 802.11a,b,g) and present the results in a meaningful way, such as in a constellation plot or a error-vector magnitude (EVM) plot.



Versions of Anritsu's Spectrum Master group of battery-operated portable spectrum analyzers, which are targeted at service personnel, reach frequencies as high as 20 GHz. Courtesy of Anritsu.

ON TMWorld.com

Product-comparison chart:
SPECTRUM ANALYZERS

The online version of this article links to a chart of currently available 2.5-GHz and up spectrum/signal analyzers. The chart lists manufacturers, model numbers, and frequency ranges and also highlights key features of each instrument.

www.tmworld.com/2007_06

Faster sweep times, which depend on RBW and can be as fast as 1 ms, add to a signal analyzer's utility. In some units, you can disable the display to also help speed up sweep times.

Depending on the signal under examination, a VSA's combination of RBW and sweep speed might capture everything of interest. But some newer modulation schemes might have key details that slip between a sweep. Addressing this demand, the real-time spectrum analyzer (RTSA) continuously examines digitized data and transforms it into the frequency or modulation domain.

An early innovator in the RTSA field was Tektronix, although other vendors indicate they are working on similar capabilities. The Tektronix DPX spectrum-processing engine performs 48,000 frequency transforms/s and updates its display 33 times/s to show frequency-domain transients as brief as 24 µs. Depending on the acquisition bandwidth (from 100 Hz to 100 MHz), the instrument's memory can store hours of data.

A key feature of the Tek RTSA is the frequency mask trigger (FMT), which can trigger the display if a certain amount of power appears at a certain frequency. Another special feature is the use of color to indicate how

often a frequency event has happened during a scan.

Evaluating analyzer specs

When shopping for a spectrum analyzer, many engineers first look at the frequency coverage. You'll find various general-purpose units that offer a low end in the kilohertz range and that extend to at least 2.5 GHz.

But given the emergence of broadband modulation, you also should consider RBW. RBW indicates the size of the window that sweeps across the frequency band. It must be wide enough to encompass the signal and its modulation but small enough to resolve narrow effects such as a low-level signal sitting near a carrier. With a given RBW, though, a fast sweep might pass by an unknown digital event before the detection system can respond to it; sweeping too slowly wastes operator time. To accommodate modern modulation techniques, RBW now sometimes exceeds 100 MHz.

A tradeoff with a wide RBW is dynamic range. Here, though, you may find it difficult to compare instrument specs, because dynamic range depends on the input signal level, frequency range, and offset from the carrier. Aeroflex's Harber said, "The definition of dynamic range is cranky and there's lots of 'specsmanship.' It measures the ability to see high and low levels without distortion, and with those last two words you must be very careful."

Keithley's Elo elaborated, "Dynamic range has many elements: third-order intercept [TOI], displayed average noise level [DANL], and phase-noise performance. 3GPP includes a standard for adjacent channel performance [ACP] that encompasses those three, and it's a good quick indicator of performance."

Engineers need to be careful when working with add-on mixers that extend an instrument's dynamic range, sometimes beyond 300 GHz, because mixers can lead to a reduction of 30 to 40 dB due to conversion losses.

Other specs to review, said Sai Yang, product manager for high-performance spectrum analyzers at Agilent Technologies, include an instrument's sensitivity for measuring low-level signals, the amplitude accuracy and the flatness of the frequency response, and the third-order intercept (TOI), which helps users determine whether distortion products are being generated internally.

Another thing to look at in analyzers is memory depth. For instance, even at a 410-MHz capture bandwidth, the Tek RTSA's 1-Gbyte of acquisition memory stores 1.7 s of signal.

The FSUP from Rhode & Schwarz combines the functionality of the company's high-end FSU-class spectrum analyzer with a pure phase-noise tester. It thus allows easy phase-noise measurements of voltage-controlled oscillators (VCOs), dielectric-resonator oscillators (DROs), or crystal-controlled oscillators (XCOs). It also measures harmonics and spurious emissions. Courtesy of Rohde & Schwarz.

Built-in PC capabilities

Many units now integrate a full PC, providing the benefits of mass storage and connectivity. The Anritsu 2781B even includes Matlab software so you can perform nonstandard analysis on captured data.

A hard disk or CD-ROM is convenient for storing measurements for later analysis. Almost all desktop and portable analyzers have various interfaces including USB, GPIB, or Ethernet. A few units, such as those from Agilent, Keithley, and Rhode & Schwarz, are also starting to incorporate LAN eXtensions for Instrumentation (LXI) capability, which is an alternative to GPIB that uses standard hardware. Further, with LXI, users can operate an instrument over the Web similar to how they use the front-panel interfaces.

Although Agilent helped initiate the LXI Consortium and has more than 60 instruments that support the standard, in the spectrum analysis area only its MXA midrange analyzer is LXI compliant.

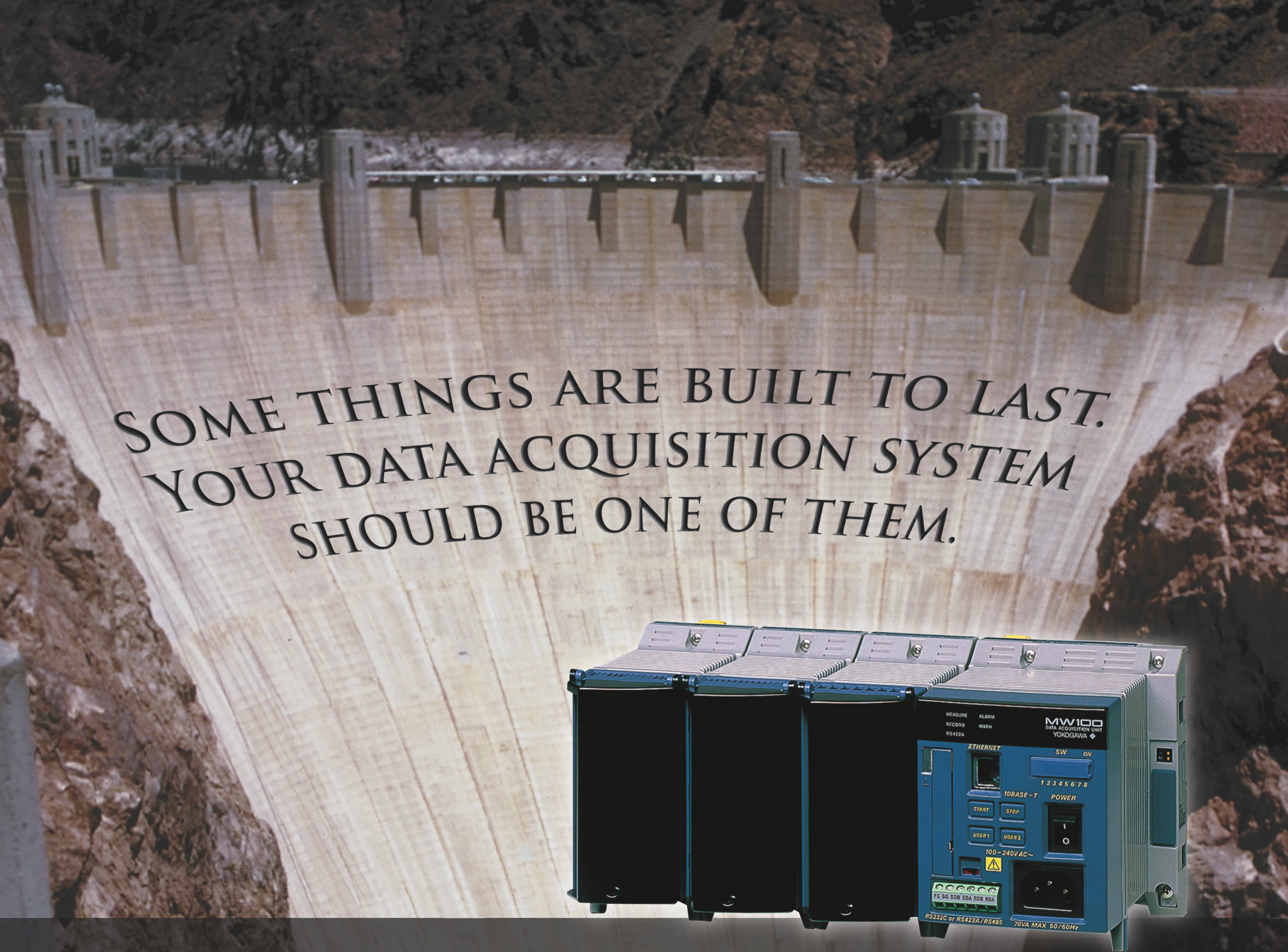
When selecting a spectrum analyzer for field use, a bright screen is an advantage. The Model 9201 from Willtek includes a high-contrast display readable in direct sunshine. Courtesy of Willtek.

(The company's high-end PSA does not yet have LXI, because the unit predates the release of the LXI standard in late 2005.) Anritsu is also on the Consortium but has focused engineering resources on other features and has yet to implement LXI connectivity, but product manager Steve Thomas said it's on the way.

More features in less space

Not surprisingly, benchtop units are becoming more powerful and more affordable, but handheld units are also improving greatly. Tom Riedl, Willtek's product manager for handheld spectrum analyzers, said, "Handhelds are coming up to near-real-time performance in terms of sweep times and display rates. They are incorporating high computational power with low power consumption and frequency ranges that rival those of desktop units. Their displays are getting better in size and contrast—after all, a great frequency range is no good if you can't use it, and displays such as ours allow viewing in direct sunlight."

In general, advances in all classes of spectrum analyzers will track new communications methods and standards. Said Tektronix's May, "In two years, we'll see different triggering capabilities and higher bandwidth. Designers will be able to see problems they've never seen before." Agilent's Yang added, "We've got the horsepower in the box; now, we have to get software to handle new formats." T&MW



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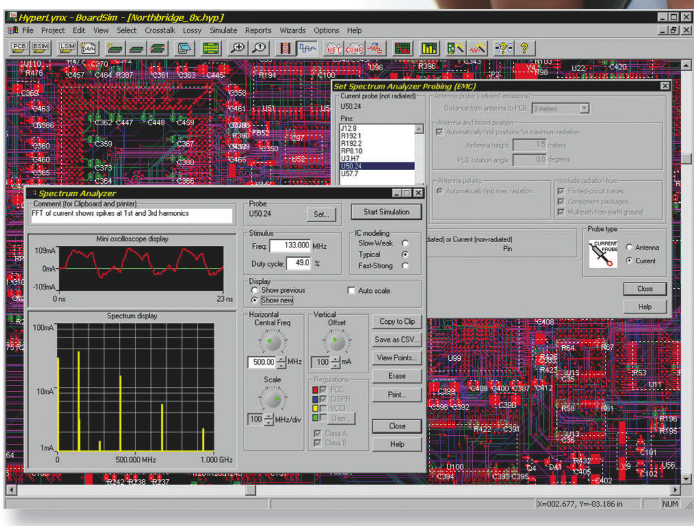

FIGURE 1. PCB modeling software can display predicted emissions using simulated oscilloscopes and spectrum analyzers. Courtesy of Mentor Graphics.

Numerical models predict EMC PERFORMANCE

BY MARTIN ROWE, SENIOR TECHNICAL EDITOR

Software that simulates PCBs, modules, and systems can uncover EMC hot spots before you build a prototype.

Preparing for electromagnetic compatibility (EMC) emissions and susceptibility tests can raise your blood pressure. Will your product pass? Following good design practices and relying on intuition for printed-circuit-board (PCB) routing, grounding, and shielding should ease some of the stress, but you can still face uncertainty as you head to the EMC lab.

To alleviate your anxiety, you can take advantage of software that models integrated circuits (ICs), PCB routing, component placement, module design, and system design. These modeling tools provide insight into how a design will perform before you commit to building a prototype.

Their simulation features let you evaluate design tradeoffs and how they can affect EMC performance. Just as EMC design is often a tradeoff between compliance, cost, and time, modeling is a tradeoff in accuracy versus complexity and simulation time.

Many circuit designers, system engineers, and EMC engineers use modeling software to predict EMC performance. In fact, EMC engineers often model a system based on assumptions or design specifications before hardware engineers develop their circuits and before PCB designers lay out their boards. In some companies, mechanical engineers use EMC modeling tools to understand how, for example, a design that optimizes cooling can adversely affect EMC.

The engineers may also work in parallel, with EMC engineers modeling a system while designers are developing circuits and PCB layouts. A system designer or EMC engineer, knowing the approximate locations of sources of electromagnetic interference (EMI) and knowing the enclosure sizes and openings, can begin to develop a system model while the PCB designer routes traces. EMC engineers often start with incomplete information and add details to their models—such as clock frequencies and rise and fall times—based on input from circuit designers as designs progress.

Engineers can also reduce EMC problems by using PCB design tools that analyze circuit designs for emissions and susceptibility. HyperLynx from Mentor Graphics, for ex-

ample, produces simulated oscilloscope and spectrum analyzer displays of currents in a PCB (**Figure 1**). The software analyzes currents in PCB interconnects and can provide emissions estimates.

Check design rules

Rule-checking software can apply design rules to a board and is one of the most useful tools available for EMC design, said Bruce Archambault, distinguished engineer at IBM. For example, a rule checker can tell you if clock signals are placed too close to the edge of a PCB or if an IC needs a decoupling capacitor.

There are several numerical methods in use today that solve Maxwell's equations and predict EMC performance. They include finite-element modeling (FEM) analysis, transmission-line method (TLM), finite-difference time-domain (FDTD) method, and others.

Commercial software programs generally take advantage of just one of the modeling methods. For example, IceWave software from Ansys uses FDTD, Comsol's Multiphysics software uses FEM, and FLO/EMC from Flomerics uses TLM. A popular paper by Dr. Todd Hubing explains these methods and the tradeoffs among them (Ref. 1). (You can also find links to additional resources on numerical EMC modeling in the online version of this article at www.tmworld.com/2007_06).

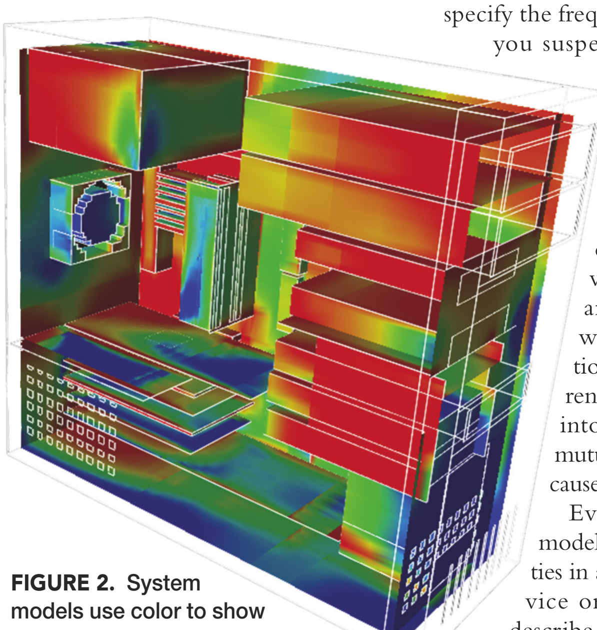

FIGURE 2. System models use color to show emissions "hot spots." Courtesy of Flomerics.

Numerical-modeling software can model the E- and H-fields surrounding a PCB in 2-D or 3-D space by solving Maxwell's equations. To solve Maxwell's equations, you must define the geometry through which fields propagate. The software applies a time-domain Gaussian pulse to the model and plots the response. A pulse introduces a wide range of frequencies to your model. You can convert the response to the frequency domain and limit your analysis to frequencies of interest.

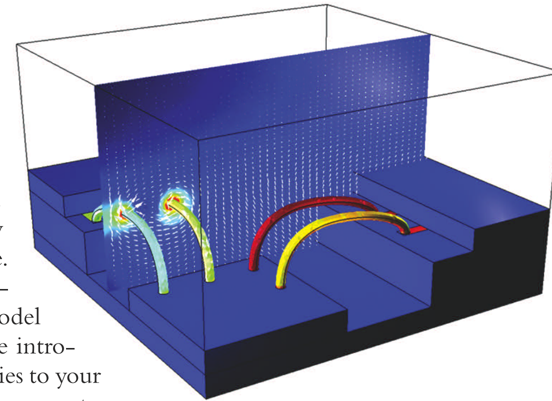

FIGURE 3. Software models of IC bond wires require information about wire geometry and materials. Courtesy of Comsol.

System models

At the system level, EMC engineers use modeling tools in which the models are based on assumptions and preliminary specifications. Initial models may contain the locations of displays, cables, and emissions sources such as power supplies and PCBs, but not much else. As designs progress, engineers will add IC locations, heat sinks, shields, and more accurate geometries from CAD software packages. EMC engineers may also get data on the materials used in a design that modeling software can use in its calculations.

Figure 2 shows a simulation of radiated emission in a computer. The image uses color to indicate field strength. Typically, red indicates the highest field-strength level. For each plot, you must specify the frequency range of interest if you suspect fields at certain frequencies such as clock frequencies or their harmonics.

EMC modeling isn't just for boards, modules, and systems, though; you can also use it at the device level. **Figure 3** shows an EMC model of bond wires inside an IC. Intentional or unintentional current in one wire can couple into adjacent wires through mutual inductance, which can cause a device to malfunction.

Even this relatively simple model highlights the complexities in accurately modeling a device or system. A model must describe the voltage between the ends of a wire (ΔV). If ΔV is greater than 0 V, then current will flow in the bond wire.

An admittance model of four wires requires that you know the properties of the materials involved. The model needs each wire's conductivity (σ), permeability (μ), and permittivity (ϵ). You then need to assign voltages to the ends of the two adjacent wires (V_1 through V_4) and calculate the current that one wire induces in the other using the matrix shown below, in which the admittance values for y_{11}, y_{22}, y_{33}, and y_{44} represent the effects that each wire has on itself. All y values are based on the values of σ, μ, and ϵ that device manufacturers provide. (Modeling software often contains a library of materials properties such as wires, enclosures, and insulators.)

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{22} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{33} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{44} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix}$$

Modeling tradeoffs

Given that a simple model can contain considerable information, you can see that modeling in such detail is impractical at the system level. Thus, EMC models often lump areas together under the assumption that the characteristics for a given area or volume are constant. These areas form a "mesh." **Figure 4** shows a mesh model for a PCB where the software creates an equivalent circuit model for each segment.

Clearly, the finer the mesh, the more accurate the system model. But that res-

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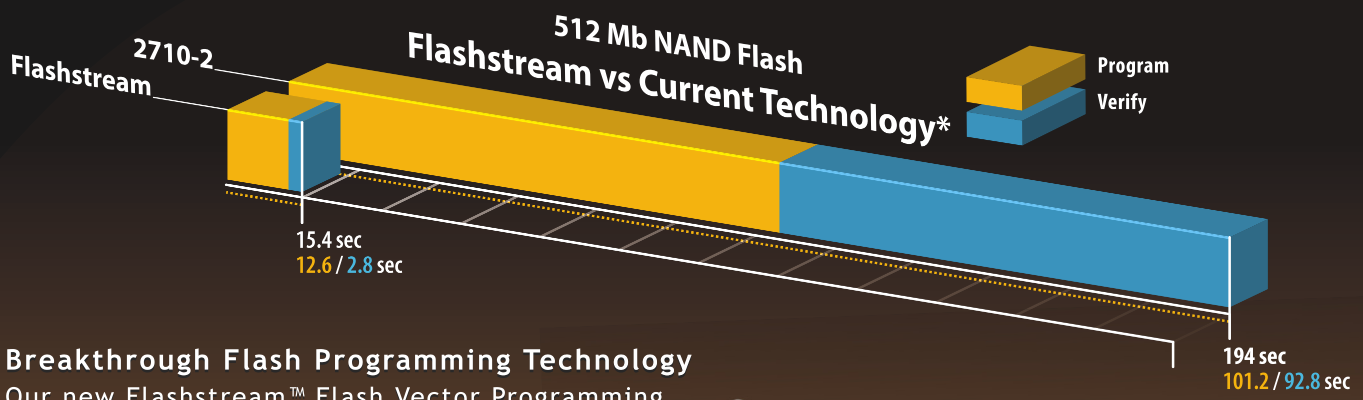

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olution comes at a price: simulation time. "A complex model may take several days to run," said Chetan Desai, IceWave product manager at Ansys. "The tradeoff is detail versus time."

Making the tradeoff decision requires experience and intuition. "You can't simulate the entire world," added Bjorn Sjodin, VP of applications at Comsol. "You must define the boundaries of what you can simulate."

When developing a model, concentrate on the areas that are most likely to cause EMC problems. At the board level, that's IC placement and trace routing. At the system level, concentrate on the location of emissions sources (ICs and oscillators) and the location of heat sinks. You also should focus on openings in an enclosure such as those for displays, controls, cables, and seams. EMC engineers can often make modeling recommendations based on experience.

Tradeoffs also occur between EMC and other parameters, particularly heat.

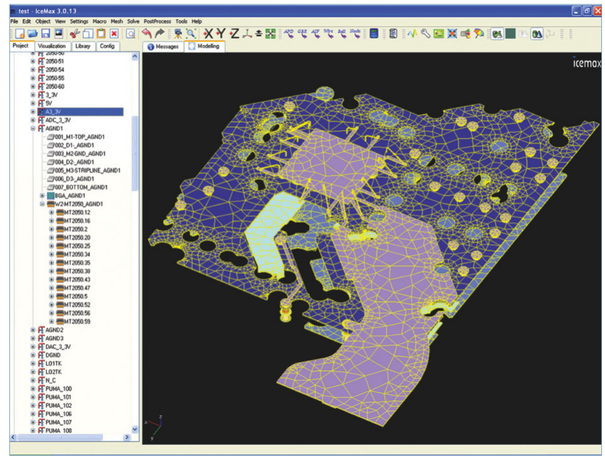

FIGURE 4. EMC models of a PCB divide the board into segments that form a mesh where each segment is modeled with an equivalent circuit. Courtesy of Ansys.

Case openings let heat escape, which makes for cooler-running components, but they also let emissions out and outside interference in. Thus, engineers often use software that simulates a system's thermal properties in conjunction with EMC simulations. "You're often faced with competing design issues," warned David Johns, VP of EM engineering at Flomerics.

Numerical EMC modeling can reduce the stress you face when testing a physical product, but it won't guarantee success in the test lab. "There's no replacement for the insight of an experienced EMC engineer," said Archambault. T&MW

REFERENCE

1. Hubing, Todd H., "Survey of Numerical Electromagnetic Modeling Techniques," University of Missouri-Rolla, 1991. www.emclab.umr.edu/pdf/TR91-1-001.pdf.


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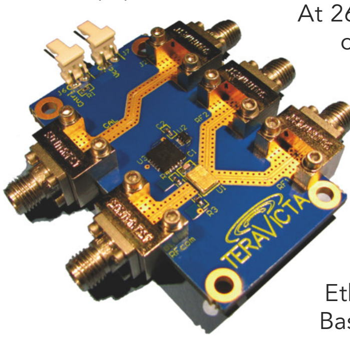
26.5-GHz SPDT MEMS switch

TeraVicta Technologies has announced a new DC to 26.5-GHz SPDT MEMS switch, the TT1244, which makes use of the vendor's MEMS manufacturing technology. The TT1244 delivers low insertion loss (from 0.1 dB at DC to 1.8 dB at 26.5 GHz) and good linearity (with third-order intercept point [IP3] at better than 75 dBm). Isolation ranges from 60 dB at DC to 20 dB at 26.5 GHz. The switch comes packaged in a standard surface-mount micro BGA.

Applications for the TT1244 include automated test equipment (ATE) and other test instrumentation. At 26.5 GHz, the device covers the K band for communications and instrumentation products, and it can test high-speed interconnect protocols such as serial rapid I/O (sRIO), PCI Express, and 10-Gbps Ethernet.



Base prices: 26.5-GHz SPDT MEMS switch evaluation board—$995; 26.5-GHz SPDT MEMS switch—$92 each in sample quantities and $49.75 each in quantities of 1000. *TeraVicta, www.teravicta.com.*

Scalable pattern-conversion software

Test Systems Strategies Inc. (TSSI) has announced two pattern-conversion software products, TD-Scan and TD-Sim. Both products can be configured to support all popular ATE platforms, performing tester rule checking for each ATE model before generating ready-to-load ATE files.

TD-Scan supports ATPG outputs with compression technologies from Cadence, Mentor Graphics, and Synopsys; it is designed to translate ATPG scan patterns in WGL or STIL format to a target ATE program format. Since scan patterns come with timing, the translation is made by a quick syntax-conversion process. For functional patterns in Verilog Change Dump (VCD) or Extended Verilog Change Dump (EVCD) format, TD-Scan can be upgraded to TD-Sim.

TD-Sim supports Verilog simulation outputs from several EDA vendors. The software is designed to translate both scan patterns and functional patterns from logic simulators in the format of VCD or EVCD event files. A waveform-based cyclization engine can automatically detect clocks and cyclize E/VCD files with a push of a button. Various filters are also available for those event files requiring conditioning before cyclization.

Base prices: TD-Scan—$5000 per year on a subscription basis; TD-Sim—$15,000 per year on a subscription basis. *Test Systems Strategies Inc., www.tessi.com.*

Network tester heads for the bench

Ixia has introduced a two-slot version of its XM12 Ethernet-based network tester: the XM2. You can use the XM2 in bench or portable applications where you need to perform network tests on protocol layers 2 through 7. The two-slot XM2 accepts the same network-interface cards as the larger XM12.

The XM2 includes an operating system for the Ixia network-interface cards. It has a removable hard drive, which makes it easier to swap operations and also increases security. Application software runs on a separate PC connected to the chassis through an Ethernet link. The XM2 runs in conjunction with IxNetwork software for testing protocol layers 2 and 3, and runs with IxLoad for testing layers 4 through 7.

Base price: $13,500. *Ixia, www.ixiacom.com.*

Edmund debuts USB 2.0 cameras

Edmund Optics has announced its EO family of intelligent machine-vision cameras with USB 2.0 interfaces. The EO family offers four combinations of resolution and speed, ranging from 752x480 pixels at 87 fps to 2560x1920 pixels at 6 fps. Lower-resolution cameras are available in monochrome or color versions, while the higher-resolution models are color-only. Each camera in the family features a progressive-scan CMOS sensor, software-based exposure control, C-mount lens fittings, and a USB 2.0 interface.

The cameras have the same 34x32x27.4-mm dimensions, allowing users to interchange cameras without needing to modify the machine-vision system.

The intelligent EO cameras come with software support that lets users adjust the frame rate by setting a specified area of interest (AOI) within the image. Frame rate can also be adjusted using binning

> > > > > > >

or subsampling. Software also allows the user to control signal gain, set exposure time, and set frame rate as well as establish trigger and digital output delays and durations. Users can set exposure, gain, and white balance manually or allow the camera to handle these parameters automatically.

The high-speed USB 2.0 interface coupled with the camera's intelligence permits the camera to provide data in a variety of modes. Software supplied with the camera allows image capture in JPEG or bitmap file formats or video capture in AVI format, both with hot-pixel correction. The camera can also perform edge enhancement, image mirroring, and image binning in both vertical and horizontal directions. Drivers for the camera are available for Microsoft's DirectShow/Windows Driver Model (WDM) and ActiveX as well as for TWAIN applications programs. In addition, a software development kit (SDK) and documentation are available.

Base price: $695 to $1195. *Edmund Optics, www.edmundoptics.com.*

Perform six safety tests

Slaughter's 6330 electrical safety tester lets manufacturers perform six common electrical safety tests: AC hipot (3.5 kV), DC hipot (3.5 kV), ground bond (30 A), insulation resis-

tance (1000 MΩ at 1000 VDC), functional run, and line leakage. The 6330 can store up to 10 test sequences with 20 steps per sequence. You can operate the instrument in single-step mode, running each test step while the instrument waits for operator input before continuing.

You can limit access to the front-panel controls to prevent an unauthorized person from accidentally choosing a wrong setting or changing the test parameters. The model 6330 can monitor minimum and maximum readings for voltage, current, power, power factor, and leakage current. You can calibrate the 6330 through the front-panel keypad, and all calibration information is stored in nonvolatile memory.

Price: $5495. *Slaughter, www.hipot.com.*

Test executive speeds sequence development

TestStand 4.0, the test executive software from National Instruments, has several new features designed to shorten test-development cycles. With version 4.0 you can drag and drop tests from a list into a sequence list. It uses reconfigurable panes instead of menus to build test sequences. And TestStand 4.0 lets you control the TestStand Engine by using what National Instruments calls "Expressions." Previous versions required you to use an ActiveX control to gain access to the software engine.

You can now perform operations such as changing the path of a LabView module with a single expression instead of using six ActiveX steps. Other enhancements include an "Output Window" that lets you post comments as a sequence runs, so you can take notes on system operation that you can use to debug test sequences. You can post error, debug, and warning messages to the development environment.

Base price: $3500. *National Instruments, www.ni.com/teststand.*

TracerDaq software goes full feature

The TracerDaq software that has been bundled with data-acquisition products from Measurement Computing is now a full-featured optional product. Unlike the bundled version, which lets you verify that your data-acquisition hardware is working, the new TracerDaq Pro provides oscilloscope, chart recorder, function generator, and rate generator applications and lets you store configurations, save data to a file for export, and change settings while an application runs.

The strip-chart recorder can log and graph data from analog, digital, counter/timer, and temperature inputs from one or more Measurement Computing instruments. It can capture samples at the maximum speed of the data-acquisition board (up to 1 million samples per channel). TracerDaq Pro also lets you trigger, on events, set alarm conditions, add comments to the signal plot, play back an acquisition, and import and plot binary and text data.

The software's oscilloscope application lets you view values acquired from analog inputs. It also samples at an instrument's maximum sample rate, triggers on an event, adds a reference or a math channel, displays measurement values for each channel, and scales channel data into engineering units.

The function generator lets you select sine, square, triangle, constant, sawtooth, or custom waveforms for analog outputs at the maximum rate of an instrument's analog output section. The software displays the sample waveform, samples per cycle, internal scan rate, and base frequency of an analog channel output signal. It can perform linear and logarithmic sweeps, change the phase, duty cycle, rate multiplier, and gate ratio of the waveform. TracerDaq Pro's rate generator lets you produce output clock signals with variable frequency, duty cycle, and initial state of the waveform.

Price: $199. *Measurement Computing, www.measurement computing.com.*

(continued)

Lambda adds 3U units to switcher line

With the introduction of 10-kW and 15-kW models in 3U rack-mount packages, Lambda now offers programmable switching power supplies in power levels from 750 W to 15 kW, output voltages from 7.5 V to 600 V, and current up to 1000 A.

Like other members of the Genesys family, the 3U 10/15-kW series includes an embedded 16-bit RS-232/485 digital interface, through which up to 31 power supplies can be daisy chained. Up to four like units can be connected in parallel and user-configured for the master to program and monitor the total current of the group. Thus, four units can appear as a single 60-kW power supply, increasing flexibility for system designers.

In addition, Genesys offers safety features, such as Safe Re-Start and Last Setting Memory. With Safe Re-Start, you can select whether the power supply returns to previous settings after power off or returns to zero (safe) output, waiting for user instructions. Last Setting Memory retains settings of output voltage and current, remote or local mode, OVP and UVL, foldback, baud rate, and start-up mode without a battery.

Lambda Americas, High Power Division, www.lambda-hp.com.

LitePoint extends ZigBee manufacturing test support

The LitePoint ZigBee software package lets you create production test programs for the manufacturing floor that allow ZigBee 802.15.4-based wireless products to be tested using existing LitePoint IQview and IQflex one-box test systems.

The IQview/IQflex includes an integrated vector signal analyzer and vector signal generator for fast test times. The ZigBee software, which is automatically recognized by the IQview/IQflex test analysis software, integrates seamlessly into the test environment, adding ZigBee test capability for both R&D and manufacturing applications.

ZigBee DUT commands are made through the chip vendor's test control interface for quick setup, while the LitePoint capture-once/measure-all hardware implementation allows full transmitter and receiver testing with very few signal captures.

The ZigBee software demodulates and displays critical transmitter measurements, like error-vector magnitude (EVM) and carrier frequency error, with the same ease and test time as basic power and spectrum measurements. For receiver testing, the IQview/IQflex internal vector signal generator sends packets to the DUT, and IQfact software calculates the packet error rate.

Price: $2200; the software is licensed on a per-use basis with site licensing available. *LitePoint, www.litepoint.com.*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GenICam shows promise

Steve Scheiber, Contributing Technical Editor

A key part of building a machine-vision system is choosing the right interface for the application: Should it be Camera Link, FireWire, GigE Vision, or some other option? In this exclusive interview, Matthew Slaughter, vision marketing engineer at National Instruments, assessed several options and also offered praise for the GenICam standard.

Q: What is the most important challenge facing today's camera standards?
A: Any worthwhile camera standard can make image acquisition easier, faster, and cheaper. While FireWire certainly provides these benefits, its maximum cable length of 4.5 m represents a serious limitation for many applications. In those applications, older analog camera technology still predominates. GigE Vision permits cable lengths up to 100 m. In the near future, I expect some combination of Firewire and GigE Vision to finally show analog the door.

Although often overshadowed by GigE Vision, the most significant camera standard in recent years may be GenICam. Sponsored by the European Machine Vision Association (www.emva.org), the GenICam programming interface formed the basis for GigE Vision and has since spread worldwide.

Q: What does GenICam add to the mix?
A: The FireWire specification defines register architectures that each camera has to follow. Such discipline is great for software interoperability but can prove too restrictive for camera manufacturers, who can't adequately differentiate their products' features. With GenICam, the cameras define themselves in XML, permitting them unique capabilities that still work with anyone's software. For example, a LabView customer can use the most advanced features of any GenICam camera without needing a specific driver for that camera.

Q: Is GenICam limited just to GigE Vision?
A: At the moment, only GigE Vision requires GenICam compliance, but GenICam XML files are appearing for FireWire cameras, and several software packages support GenICam for both FireWire and GigE Vision.

Q: How does GigE Vision compare with the other standards?
A: GigE Vision requires the system CPU to acquire and build images from packets. FireWire and Camera Link do not require nearly the same CPU overhead. To reduce this workload, companies have developed several optimization levels into their drivers. Low-level, chip-specific camera drivers can strip off image packets before the CPU ever sees them.

Matthew Slaughter
Vision Marketing Engineer
National Instruments
Courtesy of National Instruments.

Q: What changes do you see as we move forward?
A: For one thing, the 680 Mbytes/s that Camera Link offers is already too slow to cope with the next generation of sensors. Either Camera Link will have to be expanded, or the industry will need a new standard to handle the higher data rates.

One high-speed option that could be tethered or cabled is PCI Express, which would let cameras connect directly into a computer's backplane, bringing them one step closer to the processor and onboard memory. Fiber-optic cabling could allow data to travel long distances at high speeds.

We also see more intelligence moving into the camera itself. Many cameras already contain FPGAs, so why not perform image processing there as well? □

INSIDE THIS REPORT

EDITOR'S NOTE

Managing inspection data

Steve Scheiber, Technical Editor

Inspection provides considerable insight into the production process, answering questions such as how much solder gets deposited on the pads, were the correct components deposited correctly, and will the joints survive long-term service?

The value of the answers depends on what you do with them. Simply collecting data in an archive borders on the useless. You need to massage the data into information that you can apply to improving your process or modifying your product or your design.

The article on p. 71 explores data storage and analysis. In researching the topic, I discovered that in many respects, inspection systems produce too much data. An in-circuit or functional tester may report that a certain board passed or failed along with the nature of the failure if there is one. But inspection processes can record the dimensions, volume, and position of solder on every pad before putting the parts on the board; the position and shape of every part before the reflow oven; and the actual shape of every solder joint after reflow.

The key for system developers is to determine what to save, what to discard, and what to analyze so only the results are stored. More and more tools are emerging to help with this endeavor. Applying them carefully will make the inspection step far more valuable for managing your overall process. □

Contact Steve Scheiber at sscheiber@aol.com.

HIGHLIGHTS

Cognex debuts inspection sensors

The new Checker 200 inspection sensors from Cognex offer built-in lighting, a variable working distance, and inspection rates faster than 6000 ppm. The sensors can find codes printed on a label, can inspect multiple features simultaneously, and can accommodate varying part positions on a line.

All Checker 200 sensors feature an IP67 housing, quick disconnect cables, and USB connectivity. The Checker 201 handles part finding and inspection, while the Checker 202 adds ladder-logic capability to support custom configurations.

Cognex positions the Checker line within the "inspection sensors" category, which an end user can deploy to solve detection and checking problems (but not gauging). Inspection sensors typically feature simple optical and lighting configurations and generate pass/fail signals. They can replace limit switches as well as photoelectric, inductive, and other sensors.

In contrast, products in the "machine vision" category typically offer a range of optics and lighting options and generally require a systems integrator to deploy. Machine-vision systems typically generate data that must be post-processed; they solve GIGI (guidance, inspection, gauging, identification) problems. Base price: $1495. www.cognex.com.

Imperx cameras comply with GigE Vision and GenICam

Imperx has announced that its Lynx family of Gigabit Ethernet cameras is now fully compliant with the GenICam and GigE Vision standards. "Achieving this compliance for our cameras will greatly simplify our customer's development efforts," said Imperx president Petko Dinev.

The cameras are available in monochrome or color configurations, offering 8-, 10-, or 12-bits-per-pixel data under software-configuration control. The electronic shutter control offers pre-exposure and double exposure, and the shutters can be triggered through software or external signals.

Software support includes Windows and Linux drivers, development kits for C++ and Visual Basic, and support for a variety of instrument-control packages. Software tools for data acquisition and display, camera configuration, and triggering waveform generation are built in. www.imperx.com.

White paper clarifies IPC standard

The physical characteristics of lead-free solder impose new defect types that test and inspection techniques must address. For example, lead-free solder's higher melting point and reduced wetting, compared with leaded solder, encourages voids in the solder balls in lead-free ball-grid arrays. But at what point do voids move from an acceptable variation to represent a quality problem?

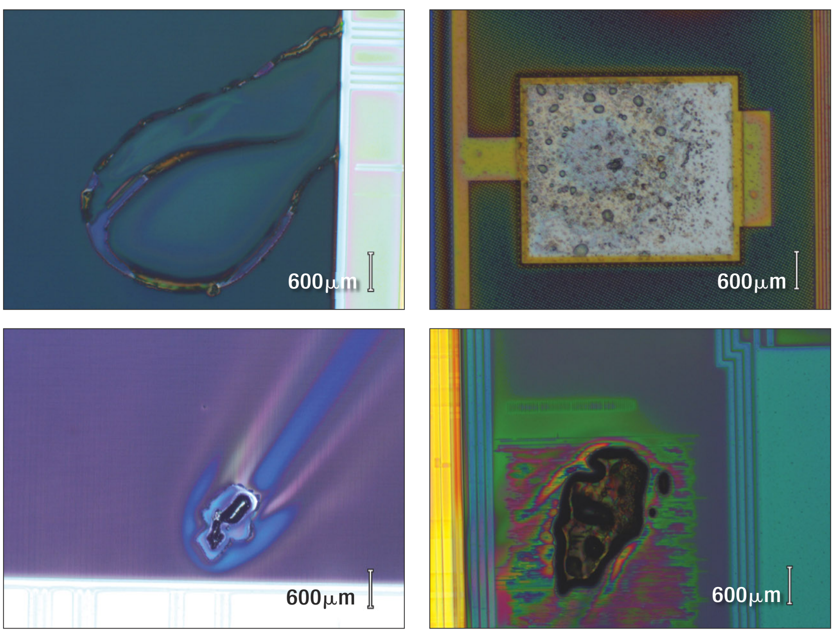
The IPC has produced a number of specifications that directly address this issue. An Agilent Technologies white paper provides a concise, readable description of one of these standards: IPC-7095A, which establishes limits on a void's percentage of ball volume and ball diameter as well as other criteria that flag situations requiring some kind of corrective action.

The standard advocates transmission or 3-D x-ray inspection as the best way to identify BGA voids both at incoming inspection and after device attachment to a PCB. Although the white paper emphasizes Agilent's x-ray inspection system, it presents general principles that do not depend on a single platform. cp.literature.agilent.com/litweb/pdf/5989-5663EN.pdf.

Image-sensor defects can ruin an image

Jon Titus, Contributing Technical Editor

When you “snap” a photo with a point-and-shoot camera or a cell phone, you hope to obtain a blemish-free image. The makers of CMOS image sensors used in these and other electronic products have a similar goal: They strive to ensure that their sensors arrive at product manufacturers free of defects. Careful inspection of sensors weeds out devices that could degrade image quality.



These four images show representative defects found in and on CMOS image sensors. Note the scale that shows these defects are relatively large. 1000 µm = 1 mm.

Because a sensor provides a light-sensitive surface, small surface defects that might not affect a purely electronic device can render a sensor chip useless. Rick Bunch, fabrication manager at Micron Technology, a manufacturer of CMOS image sensors, explained that the procedures used in the production of sensor wafers are similar to those used for devices such as NAND-flash memories and DRAM. So, most inspections in the fab look only for standard wafer-processing defects. “But after we place a color-filter array and microlens on a wafer, we perform more inspections,” said Bunch. “Any physical defects that affect the lens can cause problems.”

“We look for streaks, scratches, and particulate matter,” said Keith Chin, product-development manager at Kodak, which also produces CMOS image sensors. “And we inspect to see if the color filter or microlens has separated from the top of the sensors.” Chin described inspection as a double-edged sword, because any time you handle an image-sensor wafer, you may cause problems.

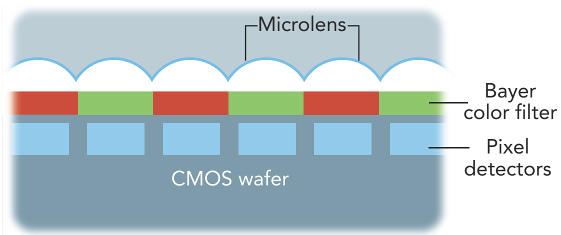
“The microlens material is soft and sticky, and the more you handle it, the worse it gets,” said Chin. “If we find particulate matter on a wafer, we will send it through a spin-rinser/dryer to remove as many particles as we can. But overall, particles are difficult to remove.” Manufacturers trace over 95% of defects on a typical megapixel sensor to particles on wafers and on glass used to encapsulate individual die (Ref 1). (See “Inspect glass, too,” p. 69.)

The individual light-sensing elements (also called pixels) on CMOS image sensors range from about 4 microns down to 2.5 microns or less on a side. “Semiconductor manufacturers strive to make pixels smaller so their customers can put image-sensor die in smaller products. Smaller pixels also let chip manufacturers put more sensors on a wafer, which reduces costs,” explained Udi Efrat, strategic marketing manager at Camtek. “But smaller pixels mean smaller defects can ruin a die.”

“Inspection equipment must find particles and other defects with dimensions as small as 3 to 5 microns,” said Carl Smets, director of the R&D group at ICOS Vision Systems. “A ‘small’ scratch used to have a width of around 10 microns, but now we must detect scratches as narrow as 2 microns.”

The need to find smaller defects means inspection equipment must provide higher-resolution images, but at almost the same speed used for lower-resolution inspections. “Say you have a given area to inspect and you raise inspection resolution by a factor of two,” said Smets. “Now, inspection equipment must acquire and process four times as much image data to inspect the same area.” Equipment from ICOS uses proprietary DSP image-processing boards the company adds as needed to keep image-processing speeds high. “Our inspection algorithms and recipes remain about the same,” said Smets. “But we use oblique illumination, which better highlights scratches and particles on image-sensor wafers.”

Unfortunately, the color filter and the microlens decrease the contrast between the surface of a sensor and any defects. The curved surface of the microlenses, for example, reflects



Not to scale

This diagram shows a cut-away side view of a color image sensor. The Bayer color filter lets specific wavelengths reach each detector. The microlens array focuses light from a scene onto individual detectors. The curved lens surface reflects light in many directions and creates a dark background during wafer inspections.

light away from a camera, so the sensor provides a dark background.

"Inspection systems find it difficult to locate dark defects on a dark surface," said Efrat of Camtek. "To overcome that problem, we use bright-field and dark-field illumination simultaneously. Bright-field lighting emphasizes differences between bright and dark areas, while dark-field lighting lets us see three-dimensional features such as particles, scratches, protrusions, and dings. These defects effectively scatter light from a low-angle dark-field light source. Some of the scattered light reaches the camera and makes defects appear bright."

"In image-sensor inspection, we need to look for light and dark defects," stressed Efrat. "We let inspection-equipment operators balance the light sources so they find all the defects important to them." In addition, Camtek applies a proprietary technique that expands the contrast information to fill the entire dynamic range available in an image.

"We also use a subpixel technique to detect defects," explained Efrat. "Normally, a defect must cover at least two adjacent pixels in an inspection image to ensure reliable detection. But subpixel resolution lets us detect defects as small as half a pixel in an image. We can apply this technique when a wafer provides a uniform background, which CMOS sensors do at low magnification. So, we can detect small defects and still run an inspection system at about four times the scanning speed needed for a higher magnification."

To overcome the dark background created by an image sensor's surface, inspection systems from Rudolph Technologies illuminate wafers with 10 to 20 times the amount of light needed to inspect a wafer of purely electronic devices. "We combine the bright illumination with standard dark-field techniques that pick up surface defects," said Rajiv Roy, marketing director in Rudolph's Inspection Business Unit. The higher magnifications needed to find small defects increase the number of images an inspection system must acquire. But the higher-power light yields a benefit: More light decreases exposure times, so a camera can spend less time at each inspection location.

(continued)

Image-sensor defects • from page 67

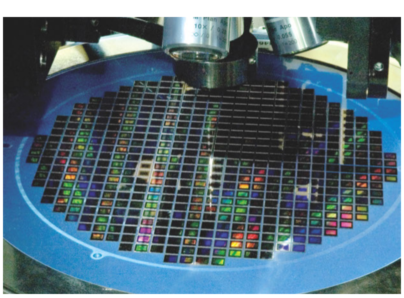
Slice, dice, and inspect

Manufacturers of CMOS image sensors often put the devices in expensive packages. To avoid assembling a damaged sensor die in a package and then discarding it after a final test, manufacturers may require inspections of sensors before and after wafer dicing. Dicing can damage die and can drop particles on their surface. "We can perform both types of inspections with little or no change-over of our inspection equipment," noted Pieter Vandewalle, director of marketing and sales for ICOS.

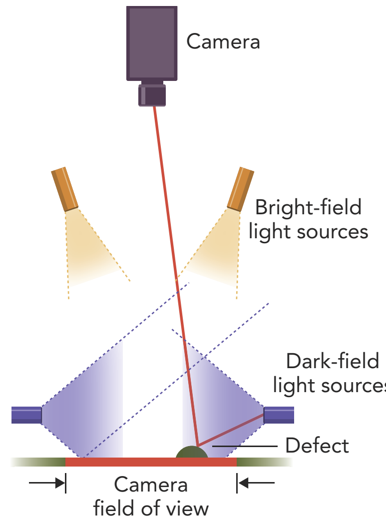
During inspections, equipment must automatically classify defects by type, size, location, and other criteria. Manufacturers set up the defect characteristics and a statistical "bin" for each defect type. Bins do not hold actual sensors, just information about the location of specific types of defects.

Because the typical defect that image-sensor manufacturers want to find has about the same dimensions as dust, wafer-inspection equipment often includes a dust removal system. "An operator can remove loose particles from a wafer prior to inspecting it," said Vandewalle. "This operation maximizes the yield of good die from each wafer."

"Sensor manufacturers want to classify defects by zones, such as the pixel array or the interconnect pads," said Amir Gilead, Camtek's VP of semiconductor inspection systems. "Zone information tells operators



Adhesive tape holds CMOS image sensors in a format called a reconstructed wafer. A tape frame stretches the material to keep it rigid. Courtesy of Camtek.



Bright-field light reflects from all surfaces, so dark defects on a dark background lack contrast. Dark-field light reflects from a wafer surface but never reaches the camera. Irregular defects do reflect this light, which reaches the camera. Defects appear as bright spots on the dark wafer.

where defects occurred, what types of defects occurred, and the algorithm that found them. Equipment operators can adjust sensitivities so an inspection system reports only defects that meet specific criteria and exist in specific zones."

A defect or a nuisance?

Most inspections that examine the optical characteristics of CMOS image sensors take place at the back end of wafer fabrication. Compared to the rest of the fab, that area does not always provide a clean environment. So, back-end inspection will detect real defects, such as embedded particles or scratches, as well as nuisance (or false) defects, such as loose surface particles or fibers. Images taken at higher magnifications reveal smaller defects, but they also reveal more nuisance defects.

"Algorithms now better distinguish between real and false defects on CMOS image sensors," noted Roy of Rudolph Technologies. "And we have augmented our inspection tools so they better classify nuisance defects automatically and ensure high wafer-processing rates." The company has recently developed a defect-classification scheme that reduces inspection costs and maintains acceptable throughput of wafers without unnecessary reclassification of nuisance defects.

Roy said, "In a clean environment, it takes less work to distinguish between true defects and nuisance defects. And much depends on the types of nuisance defects a customer has. Those 'defects' might include metal particles, organic material, fibers, and dust."

Sophisticated customers realize the value of investing in a clean environment. Others eventually learn the benefits of cleanliness. "But until they do, they tell us, 'You must make your algorithms smarter so they eliminate nuisance defects,'" explained Roy. "We put a lot of time, effort, and money into improving algorithms, but at some point we have to tell customers they might find it less expensive to invest in cleaner environments."

Reconstruct a wafer

Wafer reconstruction involves placing known-good die from several diced wafers on an adhesive material in a frame that holds the material rigid and flat. The reconstructed wafer looks similar to a whole wafer, but it lacks the round edge and unused silicon around its perimeter. In theory, a reconstructed wafer should contain only good devices. But slicing the wafer and moving die to the adhesive material could damage die or allow particles to settle on them. Thus, reconstructed wafers undergo a final inspection that creates a map that accompanies each wafer and identifies defective die.

Slight inaccuracies in pick-and-place equipment may shift or rotate die slightly when the equipment places them on an adhesive film. So, the positions of die on a reconstructed wafer may differ slightly in position and orientation from die on diced wafers. (Although the diced die are separated or "singulated," they remain in their original fixed positions.)

Camtek uses software to align an image of a die on a reconstructed wafer with a reference image stored in the company's inspection system. The

Inspect glass, too

Some image-sensor manufacturers that place sensor die in packages with a glass top use inspection equipment to examine the glass for defects. “Even if you have a perfect sensor, defects on or in the glass can cause problems,” explained Rajiv Roy, marketing director at Rudolph Technologies. (The glass above a sensor provides protection and does not substitute for the microlens materials some manufacturers apply to sensors.)

“A glass supplier inspects the glass it sells,” said Roy. “A CMOS sensor manufacturer inspects the glass after it goes on and gets bonded to a complete sensor package.” Although glass looks transparent, it may have defects such as discoloration, striations, and scratches.

“Some defects cause more problems than others,” noted Roy. A manufacturer might decide to use glass with a slight discoloration but reject glass with tiny surface scratches. Inspection-equipment operators fine-tune inspection equipment to establish which minor glass defects to accept and which to reject.

Sensor manufacturers or sensor packagers may use different package types that depend on the end use for a device. According to Roy, some packages use a single layer of glass and others use two layers separated by a vacuum. “A couple of layers of glass put particles that settle on the outer surface of the glass farther from the sensor’s focal plane. They do not affect an image as much as particles that settle close to the sensor or its focal plane.”

A high-quality sensor with an extra layer of glass costs more, but it provides a better image. “Some manufacturers that employ two layers of glass have asked us to inspect all four surfaces of the glass and to distinguish between defects on each surface,” said Roy. “In general, though, most manufacturers simply want to inspect the top surface.”—*Jon Titus*

software handles small differences in the locations of die on a reconstructed wafer and the orientation of the reference image. “This type of inspection becomes particularly important as CMOS image-sensor manufacturers produce bigger die and misalignments become larger,” said Gilead.

Inspection-equipment vendors have a vested interest in inspection results. Not only does their livelihood depend on producing good inspection results to CMOS image-sensor manufacturers, but their own equipment depends on a steady supply of high-quality cameras that use the very types of sensors they must inspect. □

REFERENCE

1. Chowdhury, Asif, “Camera Module Assembly and Test Challenges,” *Semiconductor International*, February 2006. www.reed-electronics.com/semiconductor/article/CA6302872.

How much inspection data should you save?

Steve Scheiber, Contributing Technical Editor

One difference between inspection and conventional test is the nature of the data the two processes generate. Test results can be stored as text files, spreadsheets, and the like. Inspection systems can offer similar data, but they can also measure component dimensions and solder volumes. They can even provide images of failed components or other devices so a manufacturer can trace production problems out to the field.

Images represent a new dynamic in data storage, because they take up far more space than raw data files. Pass/fail decisions can be made by pattern-

These images reflect worst-case results from a series of production runs. Courtesy of Agilent Technologies.

matching algorithms that compare two images or they can be made by a system comparing measurements on an image to a predetermined ideal.

Many manufacturers regard the archiving of every image along with the corresponding inspection results as a "given." Computer storage may seem virtually free, but all systems eventually bump up against hard limits. Even if you forego archiving the images, inspection systems can generate much more data than traditional test does.

Jeff Bishop, automated optical inspection (AOI) product manager at Agilent Technologies in Raleigh, NC, put it this way: "From our perspective, it doesn't take much longer to create a report with 70 variables than 7, but so much data often becomes overwhelming and therefore goes unused. The challenge at inspection is to provide the appropriate data at the most opportune time to help users make quick and effective decisions." So, how do you do that?

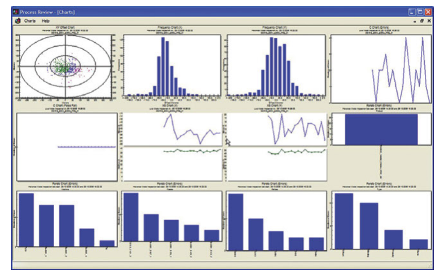
Practical considerations

Keeping every data point is like saving old magazines in case you want to read some of the articles someday. As long as the collection is small, you can probably find what you want. In a room full of magazines, however, anything that might interest you is lost in the "noise" of the surrounding clutter. If you save only individual articles, the volume of your stash increases much more slowly. And purging the pieces that you no longer want preserves your ability to locate a specific item from what remains.

Most engineers would find pruning a magazine collection far less traumatic than parting with "critical" data. And the definition of "critical" can vary dramatically depending on the application and the customer.

Product liability concerns, for example, require that a manufacturer maintain verifiable documentation that a board contained no defects when it left the factory. And legal considerations require that makers of medical and military equipment be able to trace every component in a system or subsystem back to its lot number and its original source.

This level of traceability can actually provide an economic benefit in some cases. Bishop offered an example. "Proper data tracking could reduce the cost of automobile recalls. Say an automaker discovers a bad batch of ICs in an engine-control module. Right now, they [automakers] recall every car containing that module for replacement. But if they



Looking at trends can provide more useful information than looking at the raw data. Courtesy of Agilent Technologies.

could trace the bad batch to particular board serial numbers, and if they knew the VIN numbers of the vehicles that received those boards, they could recall only the affected vehicles, drastically reducing the recall load and the associated costs."

Manufacturers of handheld devices and other commodity products may not need such tight controls. They are often more concerned about analyzing trends in the results so they can adjust their processes to increase yields and reduce rework costs.

Time sensitivity

Conventional test stations generally get boards from manufacturing delivered in batches. A production run from Tuesday may not reach in-circuit test until Wednesday. The lag between assembly and test reduces a manufacturer's ability to respond quickly to modify the production process and lower the defect rates.

Inspection, on the other hand, often occurs in-line. Bishop said that performing automated optical inspection (AOI) of solder paste after the printer step "gives you volumetric or area data in real time. You can compare the height of the deposit, its x-y position, and potentially its slope or any detected deformity against a known-good ideal. Some of that data may be useful, and some may not. Analysis

Inspection data • from page 71

could reveal that at a specific time, the paste step deposited insufficient solder volume on some (or all) solder pads. Perhaps the stencil needed cleaning. Appropriate corrections could reduce the future defect rate. Once you make the changes and achieve the corresponding improvement, there is generally no technical reason to retain all of the raw data. You track only trends, means, and extremes."

Bishop continued, "If you manufacture products in high volumes, processes change frequently in response to inspection and test data and to changes in the product or customer requirements. Except for legal considerations, the raw data loses its value after a week or 10 days. Results from pre-reflow inspection, for example, become much less valuable after the board has gone through the reflow oven."

For contract manufacturers, Bishop commented that the increased incorporation of inspection has led to different rules for what data to store and for how long. One recommendation is to adjust data life based on the cycle of delivering products to customers. "If the cycle to the customer is 45 days, for example, you may want to keep the data for 60. Data life may also depend on the types of analysis tools that you use. Data trend images and Pareto charts may need raw data from 90 or 120 days. Of course, high-reliability and high-liability situations may still require keeping at least some data forever."

Predicting future failures

Data from solder-joint inspection can help predict not only whether a board is good or bad the way test does, but whether a good board is likely to fail a few years down the road. A marginal solder joint may pass electrical test every time, but its shape may indicate a long-term problem in coping with heat or vibration or just normal wear. Process changes that result from analyzing the data using stricter criteria than mere pass/fail can help minimize the number of field failures, reducing warranty-support costs and increasing customer satisfaction.

The vast amount of data that an operation can generate during post-reflow inspection does not always need to be saved. Reducing the data "clutter" by setting priorities and determining the relevance of the data allows you to retain only trends, extremes, specific measurements, and sample runs. This approach will help you save the information you need for making effective and efficient process and product decisions. □

PRODUCTS

2-Mpixel IEEE 1394b camera

Point Grey Research has added the 2-Mpixel FL2-20S4 to its Flea2 series of IEEE 1394b cameras. The new model incorporates a Sony ICX274 1/1.8-in. progressive-scan CCD image sensor with a square pixel array and delivers 1624x1224 images at 14 fps.

The FL2-20S4 provides pixel binning and region-of-interest modes via Format_7. It also provides on-camera color processing and white balance, automatic synchronization of multiple cameras, and external trigger and strobe output. The camera comes with a C-mount lens holder and is available in monochrome and color versions. *Point Grey Research, www.ptgrey.com.*

Vision appliances

Dalsa has introduced two versions of its IPD VA3X vision appliances. The VA30 comes with Dalsa's iNspect vision-appliance software, while the VA31 includes the Sherlock machine-vision design environment.

The VA3X incorporates its processing power inside the camera controller, as opposed to the camera head, allowing users to position it alongside other controllers for easy interfacing. The dual-camera capability provides cost savings in multi-camera applications. The VA3X provides standard resolutions of 640x480 and 1024x768; resolutions to 1600x1200 are available. Base price: $3795. *Dalsa, www.goipd.com.*

5-Mpixel Camera Link camera

SVS-Vistek has added the monochrome 5-Mpixel svs625 to its SVCam camera series. The progressive-scan camera offers 2456x2058-pixel resolution, includes a 2/3-in. image sensor, and delivers 12 images/s over its Camera Link interface. In partial-scan mode, images with fewer lines can be read out at a higher speed. The camera supports 2x2-pixel binning and features a C-mount optical interface. *SVS-Vistek, www.svs-vistek.com.*

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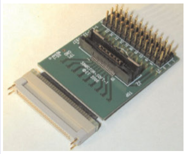
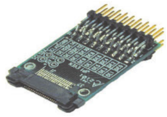

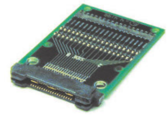
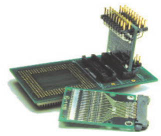

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ALEX OSCILOWSKI
COO
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Alex Oscilowski joined Rudolph Technologies as COO in November 2006, following his work as VP-strategy for the Sematech research consortium. Prior to his job at Sematech, he served as president and CEO of DFT Microsystems. Oscilowski spent his early career at Texas Instruments and Digital Equipment, and later served as president and senior VP at Kulicke & Soffa. He holds an MBA from Boston University and a BS in materials engineering from Drexel University.

Contributing editor Larry Maloney spoke with Oscilowski about industry trends in a recent telephone interview.

Answering the needs of semiconductors

Q: What are the biggest challenges facing the semiconductor industry?

A: I see three principal challenges, and they are all interrelated. First, there are the materials and process complexities that occur as the industry moves to sub-45-nm technology. That, in turn, is driving up the cost of R&D, and those expenses are forcing companies to take on a third challenge, which involves changing their business models.

Q: How are these challenges affecting suppliers of metrology and inspection equipment?

A: Before you can introduce a new material, you have to measure its critical features, which is what metrology is all about. Then, in any new manufacturing process, you also must find defects, and that is where automated macro-defect inspection comes into play. Both of these areas involve dealing with ever-increasing demands as feature sizes get smaller. At the same time, semiconductor manufacturers depend on companies like Rudolph to provide technology that will help them cope with the rising costs of R&D.

Q: Are semiconductor companies looking for suppliers that can help accelerate the sharing of data between front-end and back-end applications?

A: As process complexity increases, more customers want to do that. They are looking for better ways to manage huge amounts of data. They need to be able to identify and classify the defects in their process and then take remedial action. So, we have products like DMS Vision data-management software, which enables users to find the source of defects and manufacturing problems by bringing together all inspection, electrical test, and manufacturing information and then providing analysis. We also offer another software tool, Process Sentinel, that automatically sorts defect data and classifies wafer-level patterns. These tools are becoming a much more important service to customers as they seek to improve yields.

Q: What progress is your new AXi 935 system making in replacing micro-inspection tools?

A: Rather than replacing micro tools, the AXi system provides a complementary set of capabilities. For example, this image-based, high-throughput macro-inspection system can capture defect types that a dark-field micro tool is not able to capture. The AXi 935 builds on the tremendous success of the AXi 930 platform by offering higher throughput while still maintaining the sensitivity to detect defects down to 0.5 micron. The AXi 935 also allows customers to use a single system for a variety of applications, whether it be lithography, etch, CMP, or thin films.

Q: How has the merger last year with August Technology changed Rudolph?

A: As you look at the semiconductor industry, consolidation is certainly occurring at the chip-manufacturer level, and we are one of the companies that are undergoing such a change at the supplier level. Clearly, the merger has increased our size and scope as a vendor in the semiconductor market.

As Chairman and CEO Paul McLaughlin likes to say, this merger is a case of one plus one equaling three. From both the standpoint of higher revenues and increased capabilities, the joining of the two companies has been a huge positive. Rudolph brought its strong set of metrology offerings, while August was an established leader in automated macro-defect inspection. Both companies had excellent software products, which we have now combined in a new business unit called our data and analysis review group. So, as you look at the new company, we are in a much stronger position to be an R&D and technology provider for our customers. T&MW

Alex Oscilowski offers additional comments on R&D priorities, surface-inspection technology, and growth opportunities in the online version of this interview: www.tmworld.com/2007_06.

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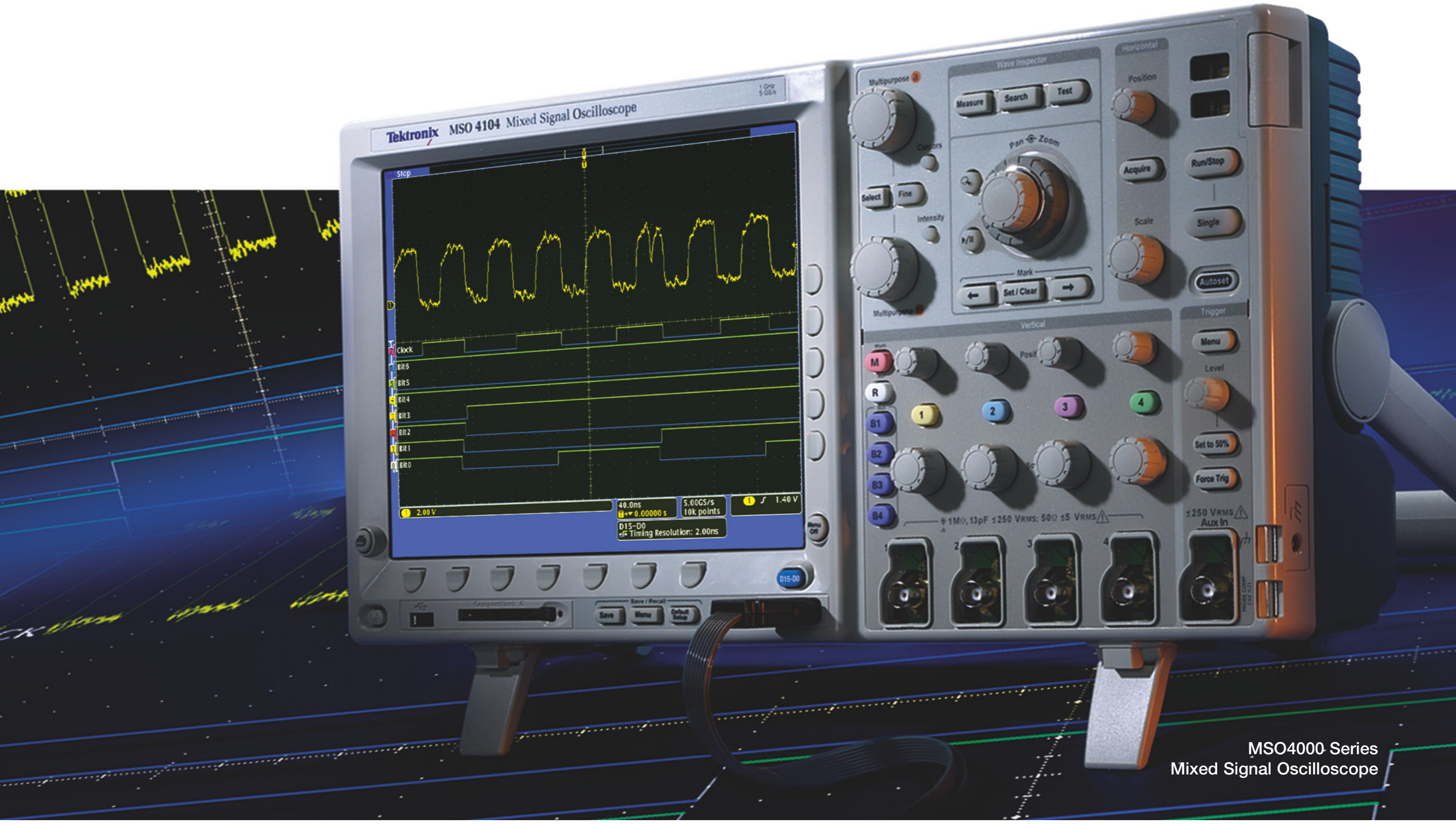

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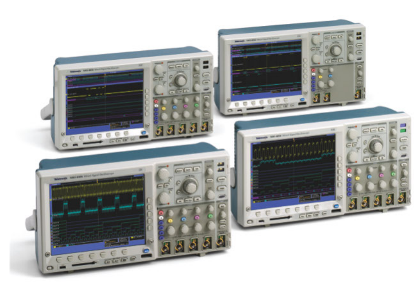

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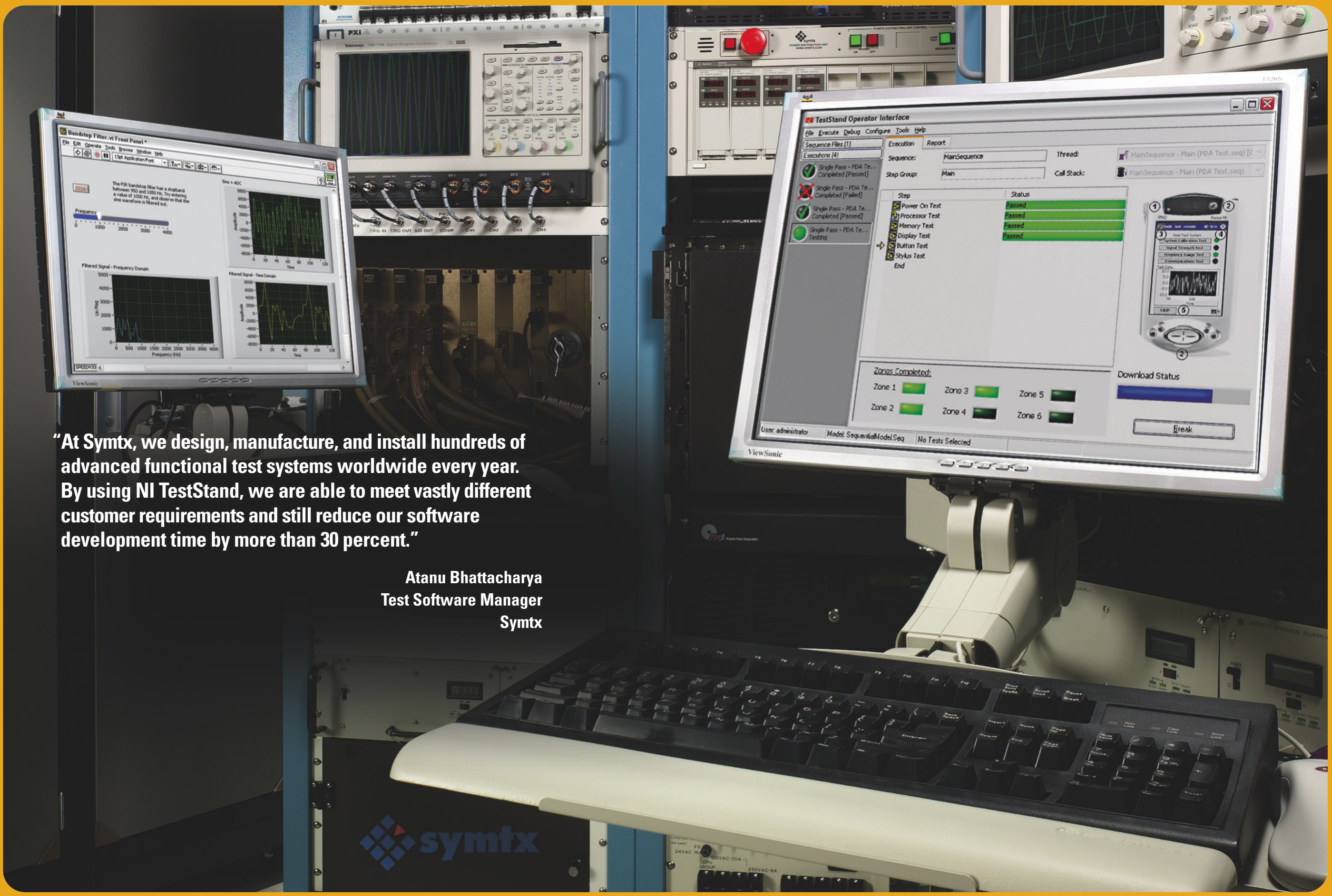

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